Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 70090

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2022.

Third Semester

Electrical and Electronics Engineering

EE 3302 – DIGITAL LOGIC CIRCUITS

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Compare TTL and ECL logic families.
2. When is Quine McClusky method preferred for logic minimization?
3. Convert the given expression to the standard SOP form.

   $F(a,b,c) = \sum m(0,1,5,6,10,11,12,13,14,15)$
4. Convert $(1001)_2$ to its equivalent Excess-3 code.
5. Differentiate mealy circuits from moore circuits.
6. Compare synchronous circuits with asynchronous circuits.
7. Distinguish between PAL and PLA
8. What are critical and non critical races?
9. What are generics in VHDL?
10. List out the objects of VHDL.

PART B — (5 × 13 = 65 marks)

11. (a) Describe the working of a 2 input ECL NOR gate.

Or

(b) Explain the operation of 2 input CMOS NAND gate.

12. (a) Implement the sum output of full adder using

(i) 4×1 multiplexer

(ii) 2×1 multiplexer

Or

(b) Design a 3 bit comparator circuit and implement using logic gates.

13. (a) Design a 2 bit even parity generator using moore circuit and implement using D flip flops.

Or

(b) Design a synchronous mod 6 counter using T flip flops.

14. (a) An Asynchronous sequential circuit is described by the following excitation and output function.

$Y = x_1 x_2 + (x_1 + x_2)y$

$z = y$

(i) Draw the logic diagram of the circuit

(ii) Derive the transition table and output map

(iii) Describe the behaviour of the circuit

Or

(b) Give the PLA realization of the given function using a PLA with 3 inputs, 4 AND gates and 2 outputs.

$F_1(a,b,c) = \sum m(0,1,3,4)$

$F_2(a,b,c) = \sum m(1,2,3,4,5)$

15. (a) Write a VHDL code to realize a half adder using

(i) behavioral modeling

(ii) structural modeling

and distinguish between both.

Or

(b) Write a VHDL code to realize a

(i) 4×1 muiltiplexer

(ii) JK flipflop

PART C — (1 × 15 = 15 marks)

16. (a) Design a switching circuit that converts a 4 bit binary code into a 4 bit equivalent gray code and implement using ROM array.

Or

(b) A clocked sequential circuit is provided with a single input x and a single output z. Whenever the input produces a string of pulses 111 or 000, the circuit should produce an output of z=1. (Overlapping is allowed)

(i) Obtain the state diagram

(ii) Obtain the state table

(iii) Design the sequence detector using D flip flop.

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Question Paper Code : 30148

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2023.

Third Semester

Electrical and Electronics Engineering

EE 3302 — DIGITAL LOGIC CIRCUITS

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is the best example of digital system?

2. Define Nibble and Byte.

3. Define Boolean algebra and Boolean Expression.

4. State De Morgan's theorem.

5. Difference between Combinational & Sequential Circuits.

6. What are the classifications of sequential circuits?

7. How can the hazards in combinational circuit be removed?

8. What is static 1 hazard?

9. What are the types of gate arrays in ASIC?

10. Give the different bitwise operators.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Draw the circuit diagram and explain the working of TTL inverter with tristate out

(ii) Explain the concept and implementation of ECL logic family.

Or

(b) (i) Explain the operation of TTL NAND gate with a neat circuit diagram. (8)

(ii) Draw the circuit of CMOS NOR gate and explain its operation. Mention any two points about the advantages of CMOS over the other digital logic families. (5)

12. (a) Obtain the minimum SOP using K-map.

$F=M_0+M_2+M_4+M_8+M_9+M_{10}+M_{11}+M_{12}+M_{13}$

Or

(b) Using 8:1 multiplexer, realize the Boolean function
T=f (w,x,y,z) = m (0,1,2,4,5,7,8,9,12,13)

13. (a) A sequential circuit has four flip flops ABCD and an input x is described by the following state equations.

$A(t+1) = (CD'+C'D)x + (CD + (CD)')x'$

$B(t+1) = A$

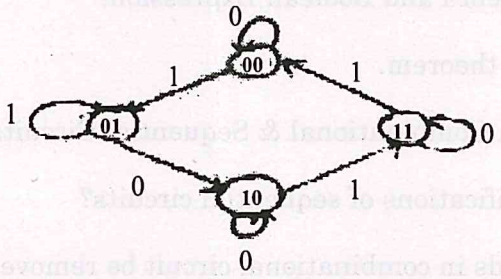
$C(t+1) = B$

$D(t+1) = C$

Obtain the sequence of states when x = 1 starting from state ABCD = 0001 Obtain the sequence of states when x = 10 starting from state ABCD = 0000

Or

(b) Design a synchronous sequential circuit using JK for the given state diagram.



14. (a) Develop the state diagram and primitive flow table for a logic system that has two inputs S and R and a single output Q. The device is to be an edge triggered SR flip-flop but without a clock. The device changes state on the rising edges of the two inputs. Static input values are not to have any effect in changing the Q output.

Or

(b) Design an asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z. The output is to remain a 0 as long as X_1 is a 0. The first change in X_2 that occurs while X_1 is a 1 will cause a Z to be a 1. Z is to remain a 1 until X_1 returns to 0. Construct a state diagram and flow table. Determine the output equations.

15. (a) Write a VHDL module that implements a full adder using an array of bit-vectors to represent the truth table.

Or

(b) (i) Write HDL behavioral description of JK flipflop using if- else statement based on value of present state. (8)

(ii) Draw the logic diagram for the following module. (5)

```
module seqcrt (A,B,C,Q,CLK);
input A,B,C,CLK;
output Q: reg Q,E;
always @ (Posedge CLK) begin E<= A&B;
Q <=E / C;
end end module
```

PART C — (1 × 15 = 15 marks)

16. (a) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the circuit are

$$Y_1 = X_1 + X_1Y_2' + X_2Y_1 \; Y_2 = X_2 + X_1Y_1' \; Y_2 + X_1Y_1, \; Z = X_2 + Y_1$$

(i) Draw the logic diagram of the circuit. (5)

(ii) Derive the transition table and output map. (5)

(iii) Obtain a flow table for the circuit. (5)

Or

(b) Design an asynchronous binary toggle circuit that changes state with each rising edge of clock input. Assume the initial output as zero.

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Question Paper Code : 20975

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2023.

Third Semester

Electrical and Electronics Engineering

EE 3302 — DIGITAL LOGIC CIRCUITS

(Common to PTEE 3302 for B.E. (Part-Time) First Semester – Regulations 2023)

(Regulations 2021)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State advantages and disadvantages of TTL.
2. Find the octal equivalent of hexadecimal number $(2F.C4)_{16}$.
3. Simplify the given Boolean expression. $(AB + CD) \cdot \left[\left(\overline{A} + \overline{B}\right) \cdot \left(\overline{C} + \overline{D}\right)\right]$.
4. Draw the circuit of the half subtractor and write its truth table.
5. Define race around condition.
6. State the rules for state assignment.
7. What are the drawbacks in designing asynchronous sequential logic circuit?
8. Why the input variables to a PAL buffered?
9. What is data flow modelling in VHDL?
10. Write the VHDL code for a logic gate which gives high output only when both the inputs are high.

PART B — (5 × 13 = 65 marks)

11. (a) (i) How can the expression, Y = (A + B).C be implemented using NAND gates? (5)

(ii) Perform addition for (205+569) using BCD addition. (4)

(iii) Convert the decimal numbers $(31)_{10}$ and $(2,988)_{10}$ into hexadecimal. (4)

Or

(b) (i) Draw the MOS logic circuit for NOT gate and explain its operation. (7)

(ii) Compare Totem pole and Open collector outputs (6)

12. (a) (i) Minimize the fundamental product of sums expression

$$Y = (A + \overline{B} + C) \cdot (\overline{A} + B + C) \cdot (\overline{A} + B + \overline{C}) \cdot (\overline{A} + \overline{B} + C) \cdot (\overline{A} + \overline{B} + \overline{C})$$

first using Boolean algebra and then by using a Karnaugh map. Then draw the circuit which implements the minimized form of Y. (9)

(ii) Simplify the logic function F in the two following cases :

(1) $F(A, B, C) = \min(1, 3, 4, 7)$

(2) $F(A, B, C) = \min(1, 3, 4, 7) + x(2, 5)$, where the don't care terms are represented by x. (4)

Or

(b) (i) Implement the product-of-sums Boolean function expressed by π (1, 2, 5) by a suitable multiplexer. (8)

(ii) Implement the function using decoder

F (p, q, r, s) = $\sum$ (0, 1, 2, 4, 7, 10, 11, 12). (5)

13. (a) For the specified state diagram shown in Figure 1 design a synchronous sequential circuit using D–FF. (13)

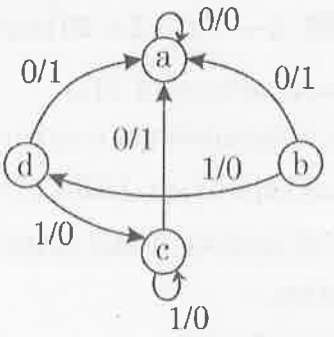

Figure 1

Or

(b) Design a synchronous mod 12 counter using NAND gates and T flip-flops. (13)

14. (a) Analyze the pulse mode circuit shown in figure 2 and derive its flow table. Also plot its state diagram. (13)

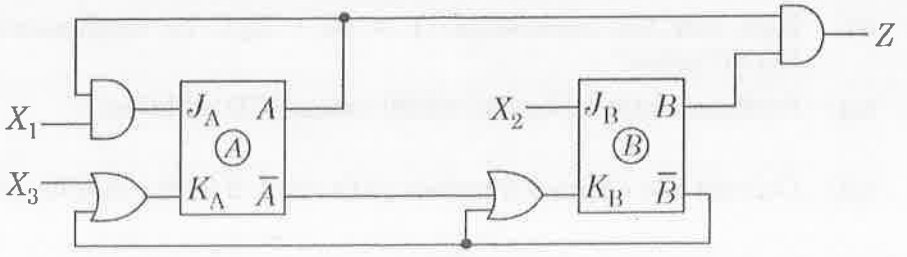

Figure 2

Or

(b) (i) Implement the following using PROM. (9)

$$A(X,Y,Z) = \Sigma_{Max}(1,2,4,6)$$
$$B(X,Y,Z) = \Sigma_{Max}(0,1,6,7)$$
$$C(X,Y,Z) = \Sigma_{Max}(2,6)$$

(ii) What is a Hazard? Brief on its types. (4)

15. (a) (i) Write a VHDL program for 1 to 4 Demux using dataflow modelling. (8)

(ii) Write short notes on built – in operators used in VHDL programming. (5)

Or

(b) Explain in detail the RTL design procedure. (13)

PART C — (1 × 15 = 15 marks)

16. (a) Obtain a set of prime implicants for the Boolean expression. (15)

$f = \Sigma_{Max}$ (0, 1, 6, 7, 8, 9, 13, 14, 15) using a table method.

Or

(b) (i) Design a BCD adder circuit capable of adding BCD equivalents of two-digit decimal numbers. Indicate the IC type numbers used if the design has to be TTL logic family compatible. (11)

(ii) For the given Boolean expression, $Y = \overline{(A \cdot B) + (C \cdot D)}$. Draw the circuit and write the truth-table. (4)

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Question Paper Code : 51008

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2024.

Third Semester

Electrical and Electronics Engineering

EE 3302 — DIGITAL LOGIC CIRCUITS

(Common to PTEE 3302 – Digital Logic Circuits for B.E. (Part-Time) First Semester – Electrical and Electronics Engineering – Regulations 2023)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert the number $(255)_{10}$ in to binary format.
2. What is the largest binary number that can be expressed with 7 bits? What is its equivalent decimal value?
3. Draw 8 × 1 multiplexer using only 4 × 1 multiplexers.
4. State any two differences between Multiplexer and Demultiplexer.
5. The output Qn of a JK flip-flop is zero. It changes to 1 when a clock pulse is applied. What are the inputs at J and K?
6. List down the terminal count of a 8 bit binary counter in up-mode and down-mode.
7. Sketch the generic architecture of CPLD.
8. Justify the statement, "Race around condition that exist in flip flops can be eliminated".
9. When can RTL be used to represent digital systems?
10. Write VHDL code for half adder in data flow model.

PART B — (5 × 13 = 65 marks)

11. (a) (i) What are the applications of Gray code? (4)

(ii) Convert the following numbers into Gray code numbers.

$(89)_{10}$

$(54)_{16}$

$(145)_8$ (9)

Or

(b) Given the 8-bit data word 11000100, generate the 13-bit composite word for the Hamming code that corrects single errors and detects double errors.

12. (a) Use Quine-McCluskey principle to simply the following expression $f = \sum m(1, 2, 3, 5, 6, 7, 8, 9, 12, 13, 15)$ and implement using logic Gates.

Or

(b) Design a 4-bit gray to binary code converter using K-map.

13. (a) With a neat diagram explain the working of bidirectional shift register.

Or

(b) Design and draw the logic diagram of Mod-12 synchronous counter using JK flip-flops.

14. (a) Design a circuit with optimum utilization of PLA to implement the following functions $F1 = \sum m(0, 2, 5, 8, 9, 11)$, $F2 = \sum m(1, 3, 8, 10, 13, 15)$, $F3 = \sum m(0, 1, 5, 7, 9, 12, 14)$.

Or

(b) Implement a full adder using PAL and ROM.

15. (a) Write an HDL dataflow description of a 4-bit adder, subtractor of unsigned numbers. Use the conditional operator.

Or

(b) Develop a VHDL code for Binary UP/ DOWN counter using JK flip flops.

PART C — ($1 \times 15 = 15$ marks)

16. (a) Derive the PLA programming table for a combinational circuit that squares a 4-bit number and minimize the number of product terms. What is the width of the output?

Or

(b) A synchronous sequential machine has a single control input x, the clock and two Outputs A and B. On consecutive rising edges of the clock, the code on A and B changes from 00 to 01 to 10 to 11 and repeats itself if $x = 1$; if at any time $x = 0$, it holds to the present state. Draw the state diagram, design and implement the circuit using T flip flop.