

UNIT I PN JUNCTION DEVICES

9

PN junction diode –structure, operation and V-I characteristics, diffusion and transition capacitance - Rectifiers – Half Wave and Full Wave Rectifier,– Display devices- LED, Laser diodes, Zener diodecharacteristics- Zener Reverse characteristics – Zener as regulator

Introduction:

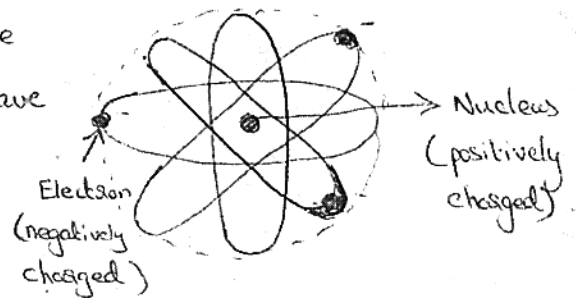
An electronic device controls the movements of electrons. The study of electronic devices requires a basic understanding of the relationship between electrons and the other components of an atom.

Atomic Theory:

The atom:

The atom can be thought of as consisting of a central nucleus surrounded by orbiting electrons as shown below. Thus it may be compared to a planet with orbiting satellites. Satellites are held in orbit by the attractive force of gravity due to the mass of the planet, so each electron is held in orbit by an electrostatic force of attraction between it and the nucleus.

Each electron has a negative electrical charge of 1.602×10^{-19} Coulombs. and some particles within the nucleus (protons) have a positive charge of the same magnitude. Since opposite charges attract, a force of attraction exists between the oppositely charged electron and nucleus.



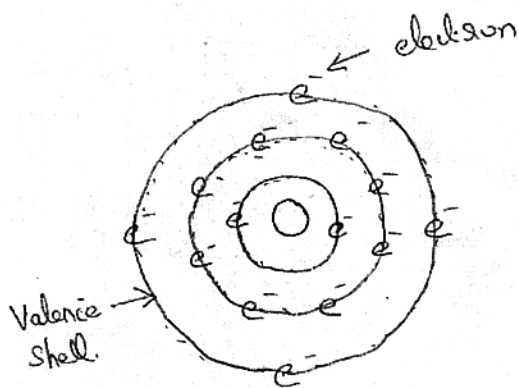
The nucleus of an atom is largely a cluster

(2)

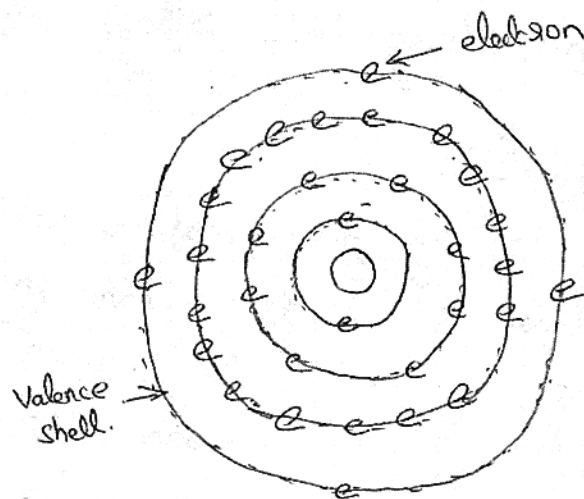
The atomic weight is approximately equal to the number of protons and neutrons in the nucleus of the atom. The atom of the semiconductor material Silicon has 14 protons and 14 neutrons in its nucleus as well as 14 orbital electrons. Therefore, the atomic number for Silicon is 14, and its atomic weight is approximately 28.

ELECTRON ORBITS AND ENERGY LEVELS:-

Atoms may be conveniently represented by the two-dimensional diagram shown below. The electrons in the outer shell determine the electrical characteristics of each particular type of atom. These electrons are usually referred as valence electrons.



(a) Silicon atom



(b) Germanium atom

The atoms represented above are those of two important semiconductor materials, Silicon (Si) and Germanium (Ge). It is seen that each of these atoms has four electrons in a valence shell that can contain a maximum of eight. Thus the valence shells have four electrons and four holes. A hole is defined as an absence of an

(3)

easily moved by the application of relatively small amount of energy. Much large amount of energy must be applied to easily moved move an electron in the valence band.

Conduction in Solids:

Electron Motion and Hole Transfer:

Conduction occurs in any given material when an applied voltage causes electrons within the material to move in a desired direction. This may be due to one or both of two processes, electron motion and hole transfer. In electron motion, free electrons in the conduction band are moved under the influence of applied electric field, thus creating an electric current. Hole transfer involves electrons which are still attached at atom.

If some of the electron positions in the valence shell of an atom are not occupied by electrons, these are holes where electrons could exist. When sufficient energy is applied an electron may be made to jump from one atom to a hole in another atom. When it jumps the electron leaves a hole behind it. and thus the hole has moved in a direction opposite to that of the electron.

Since the flow of electric current is constituted by the movement of electrons and holes, electrons and holes are referred to as charge carriers. Each time a hole moves, an electron must be supplied with sufficient

Semiconductor :-

Semiconductor atoms normally have four outer shell electrons and four holes and are so close together that the outer shell electrons behave as if they were orbiting in the valence shells of two atoms. In this way each valence shell electron fills one of the holes in the valence shell of a neighbour atom. This produces an atomic bonding force known as covalent bonding.

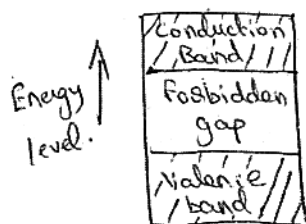
In fact some of the electrons are so weakly attached to their atoms that they can be made to break away to create a current flow when a voltage is applied.

Insulator :-

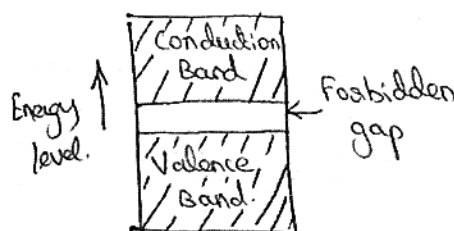
In insulating materials the atoms bond together in a similar way to semiconductor (covalent bonding). But the valence shell electrons are so strongly attached to their atoms in an insulator that no charge carriers are available for current flow.

Energy Bands in Different Materials :-

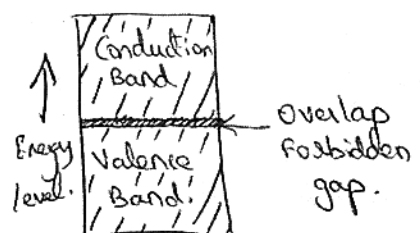
The energy band diagram shows that insulators have a wide forbidden gap, semiconductors have a narrow forbidden gap and conductors have no forbidden gap at all.



(a) Insulator



(b) Semiconductor



(c) Conductor

N-Type and p-Type Semiconductors:

Doping:

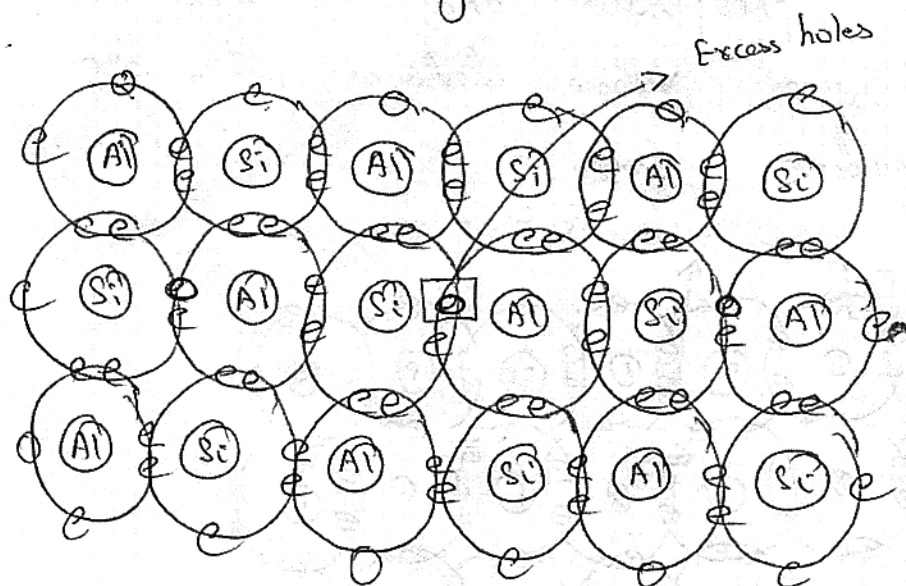
Pure Semiconductor material is known as intrinsic material. Before intrinsic material can be used for device manufacture, impurity atoms must be added to improve its conductivity. The process of adding the atom is termed doping. Two different types of doping are possible namely donor doping and acceptor doping.

The donor doping generates free electrons in the conduction band and acceptor doping produces valence band holes or a shortage of valence electrons in the material. After doping the semiconductor is known as extrinsic material.

N-Type MATERIAL:

In donor doping the pentavalent atom is added to the undoped material. The impurity atoms form covalent bonds with the silicon or germanium atom because the semiconductor atoms have only four electrons in their valence shells, there is one extra valence shell electron for each impurity atom added. Each electron's additional electron produced in this way enters the conduction band as a free electron. It is shown in below fig where there is no hole for the fifth electron from the outer shell of the impurity atom therefore this electron

Since holes can be said to have a positive charge acceptor doped semiconductor material is referred to as p-type material. Typical acceptor materials are boron, aluminum and gallium.



P-type Semiconductor.

There are many more electrons than holes in n-type material, so electrons are said to be the majority charge carriers and holes are said to be minority carriers in n-type material. In p-type material holes are the majority carriers and electrons are minority carriers.

Effects of Heat

When a conductor is heated, it will have positive temperature coefficient of resistance (ie) its resistance increases with increasing the temperature.

In case of semiconductor current increase with increasing temperature therefore semiconductors will

Semiconductor materials are shown side by side representing a p-n junction as shown below.

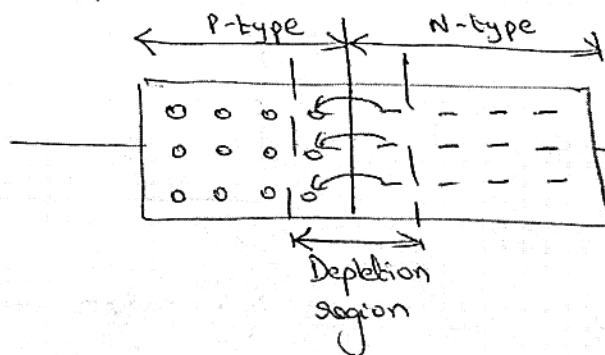


fig. PN junction diode.

Holes and electrons are close together at the junction.

So some free electrons from the n-side are attracted across the junction to fill adjacent holes on p-side. They are said to diffuse across the junction from a region of high carrier concentration to one of low concentration.

Barrier Voltage:-

The n-type and p-type materials are both electrically neutral before the charge carriers diffuse across the junction. When negative ions are created on the p-side, the portion of the p-side close to the junction acquires a negative voltage. Similarly the positive ions created on the n-side gives the n-side a positive voltage close to the junction.

Thus the negative voltage on the p-side tends to repel additional electrons crossing from the n-side. Similarly positive voltage on n-side tends to repel any additional ^{holes} electrons crossing from the p-side. The initial diffusion of charge carriers creates a barrier voltage at the junction. The typical value of barrier

Reverse Biased:-

When an external bias voltage is applied to a pn junction, positive to the n-side and negative to the p-side, electrons from the n-side are attracted to the positive terminal and holes from the p-side is attracted to the negative terminal.

As shown in fig. holes on the p-side of the junction are attracted away from the junction on the n-side. This causes the depletion region to be widened and the barrier voltage to be increased. With the barrier voltage increase there is no possibility of majority carrier current flow across the junction. and the junction is said to be reverse biased. Because only a very small reverse current flows a reverse biased pn junction can be said to have a high resistance.

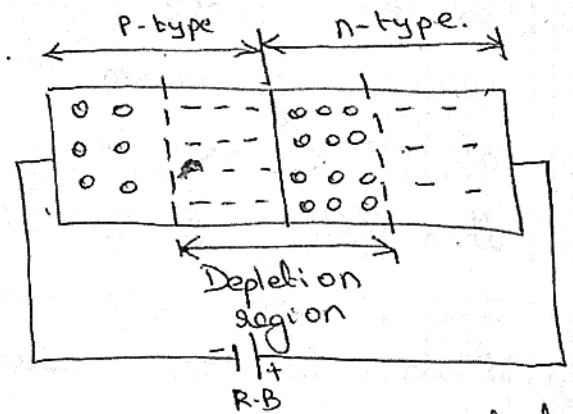


fig. Reverse Bias applied to PN junction.

Although there is no possibility of a majority charge carrier current flowing across a reverse-biased junction, minority carriers generated on each side can still cross the junction. This reverse saturation current is normally a very small quantity ranging from nanoamps to microamps, depending

is dc. This resistance is denoted as R_F and defined as the ratio of applied dc. voltage to dc. current

$$R_F = \frac{V_F}{I_F}$$

Advantages:-

1. It is very much compact and portable.
2. It can be used as ON-OFF switch.
3. It is operated with low voltage and has low power consumption.

Disadvantages:-

1. It is temperature sensitive.
2. There is a time delay in switching ON-OFF hence it is not suitable for high speed operations.
3. Due to large reverse current, noise level is high.

Applications:-

It is used in.

1. Rectifiers circuits
2. clipper and clamper circuits
3. Voltage multiplier circuits.

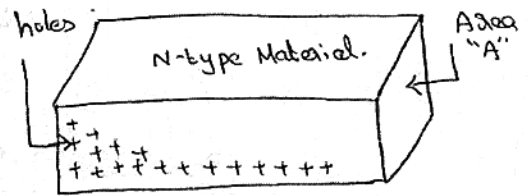
Drift Current:-

When an electric field is applied across the semiconductor material, the charge carriers attain a certain drift velocity v_d , which is equal to the product of the mobility of the charge carriers and the applied electric field intensity, E . The holes move towards the negative terminal of the battery and the electrons move towards the positive terminal.

if either electrons or holes is greater in one region of a semiconductor as compared to the rest of the region. In a semiconductor material, the charge carriers have the tendency to move from the region of higher concentration to that of lower concentration of the same type of charge carriers. Thus the movement of charge carriers takes place resulting in a current called diffusion current. The diffusion current depends on the material of the semiconductor, types of charge carriers and the concentration gradient.

Diffusion current density due to holes, J_p is given as

$$J_p = -q D_p \frac{dp}{dx} \text{ A/cm}^2$$



Similarly the diffusion current density due to the free electrons, J_n is given by

$$J_n = q D_n \frac{dn}{dx} \text{ A/cm}^2$$

where $\frac{dn}{dx}$ and $\frac{dp}{dx}$ are the concentration gradients for electrons and holes respectively and D_n, D_p represents the diffusion coefficient expressed in cm^2/s for electrons and holes.

Transition Capacitance (C_T)

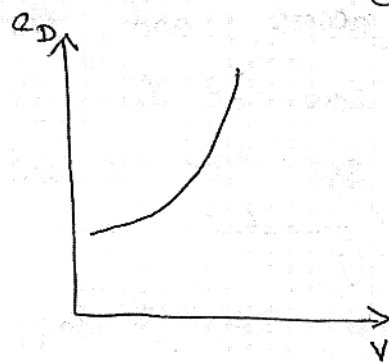
When a diode is reverse biased, reverse current flow due to minority carriers. The majority charged particles i.e. electrons in n-region and holes in p-region move away from the junction. This increases the width of the depletion region.

$$C_D = \frac{dQ}{dV}$$

The diffusion capacitance can be determined by.

$$C_D = \frac{\tau I}{\eta V_T}$$

where τ = Mean life time for holes.



P-N Diode Switching Characteristic:-

* Diode reverse recovery time:

When an external voltage forward biases a p-n junction, the steady state density of minority carriers is shown below. The number of minority carriers is very large. These minority carriers have in each case been supplied from the other side of the junction, where being majority carriers they are in plentiful supply.

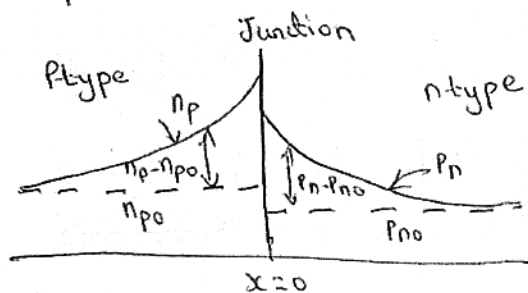


Fig. a. Forward biased junction.

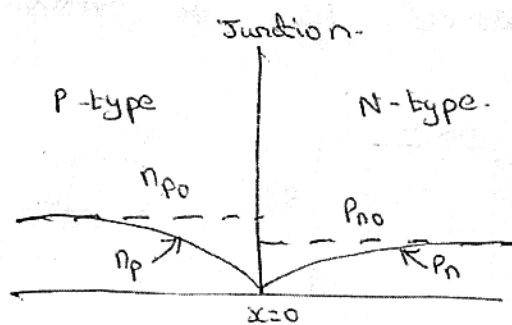


Fig. b. Reverse biased junction

When an external voltage reverse biases the junction the steady state density of minority carriers as show above. Fig. b. Far from the junction the minority carriers are equal to their thermal equilibrium values p_{no} and n_{po} . As the minority carriers approach the junction they are rapidly swept

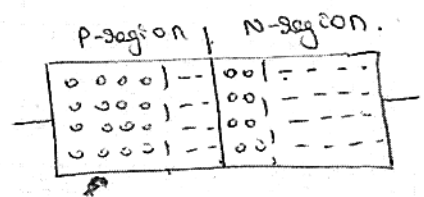
Diode Current Equation:-

(12)

The diode current includes both the hole current due to the movement of holes from p-side to n-side and electron current due to the movement of electron from n-side to p-side.

$$\therefore I = \text{hole current into n-side} + \text{electron current into p-side} \quad \text{--- (1)}$$

The hole concentration of n-region under open circuit condition at the junction is



$$p_n(0) = p_{n0} e^{V_0/V_T} \quad \text{--- (2)}$$

where p_{n0} is hole concentration of n-region under thermal equilibrium.

When the forward bias voltage V , is applied across the junction the hole concentration of the n-region becomes

$$p_n(0) = p_{n0} e^{V/V_T} \quad \text{--- (3)}$$

Under forward bias condition, the excess hole from the p-region diffuses into n-region. Thus the hole concentration injected p-side to n-side is.

$$p_n(0) = p_n(0) - p_{n0} \quad \text{--- (4)}$$

Substitute equ (3) in equ (4), we get.

$$\begin{aligned} p_n(0) &= p_{n0} e^{V/V_T} - p_{n0} \\ &= p_{n0} [e^{V/V_T} - 1] \quad \text{--- (5)} \end{aligned}$$

In general the hole concentration injected from p-side to n-side for any depletion width, x is

Considering the carrier generation and recombination the depletion region of different materials the general diode current equation is (12)

$$I = I_0 \left[e^{\frac{V}{\eta V_T}} - 1 \right] \quad \text{--- (12)}$$

where
 $\eta = 1$ for germanium
 $\eta = 2$ for silicon.

Under reverse bias, the diode current is given as

$$I = I_0 \left[e^{-\frac{V}{\eta V_T}} - 1 \right] \quad \text{--- (13)}$$

Problem:-

- i) The reverse saturation current of a germanium PN junction diode is $6 \mu A$. Calculate the current flow through the diode when the applied forward bias is $0.2 V$ at room temperature.

Given Data:-

$$I_0 = 6 \mu A ; V = 0.2 V ; T = 300 K \text{ for Ge ; } \eta = 1$$

w.k.t. $I = I_0 \left[e^{\frac{V}{\eta V_T}} - 1 \right]$

$$V_T = \frac{T}{11600} = \frac{300}{11600}$$

$$\therefore I = 6 \times 10^{-6} \left[e^{\frac{0.2 \times 11600}{300}} - 1 \right]$$

$$\boxed{I = 13.6 \text{ mA}}$$

Assignment :-

1. Calculate the silicon diode current for the forward bias voltage of $0.6 V$ at $25^\circ C$ if the reverse saturation current is $10 \mu A$.
 (Ans. $1.18 A$)

diode becomes more positive with respect to the cathode (14)
and hence diode D conducts. For an ideal diode the forward voltage drop is zero. So the whole input will appear across the load resistance R_L .

During negative half cycle of the input signal, the anode of the diode becomes negative with respect to the cathode and hence diode "D" does not conduct. For an ideal diode, the impedance offered by the diode is infinite. So the whole input voltage appears across the diode D. Hence the voltage drop across R_L is zero.

Ripple factor :- (Γ)

The ratio of rms value of a.c component to the d.c component in the output is known as ripple factor.

$$\Gamma = \frac{\text{rms value of a.c Component}}{\text{d.c. value of Component}} = \frac{V_{r, \text{rms}}}{V_{dc}} \quad \dots (1)$$

where $V_{r, \text{rms}} = \sqrt{V_{\text{rms}}^2 - V_{dc}^2}$

Substitute $V_{r, \text{rms}}$ in equ (1) and rearrange it we get.

$$\Gamma = \frac{\sqrt{V_{\text{rms}}^2 - V_{dc}^2}}{V_{dc}} = \sqrt{\frac{V_{\text{rms}}^2}{V_{dc}^2} - \frac{V_{dc}^2}{V_{dc}^2}}$$

$$\Gamma = \sqrt{\frac{V_{\text{rms}}^2}{V_{dc}^2} - 1} \quad \dots (2)$$

The d.c content of the voltage across the load and is given by

rearrange the above expression we get.

$$I_{dc} R_L + I_{dc} [r_f + r_s] = \frac{V_m}{\pi}$$

$$I_{dc} [R_L + r_f + r_s] = \frac{V_m}{\pi}$$

$$I_{dc} = \frac{V_m}{\pi [R_L + r_f + r_s]} \quad \dots \textcircled{6}$$

The rms voltage value of the load resistance is given as

$$V_{rms} = \left[\frac{1}{2\pi} \int_0^\pi V_m^2 \sin^2 \omega t \, d(\omega t) \right]^{1/2}$$

$$= \left[\frac{V_m^2}{2\pi} \int_0^\pi \sin^2 \omega t \, d(\omega t) \right]^{1/2}$$

$$\text{w.k.t. } \sin^2 \theta = \frac{1 - \cos 2\theta}{2}$$

$$= \left[\frac{V_m^2}{2\pi} \int_0^\pi \frac{[1 - \cos 2\omega t]}{2} d(\omega t) \right]^{1/2}$$

$$= \left[\frac{V_m^2}{4\pi} \left[\int_0^\pi d(\omega t) - \int_0^\pi \cos 2\omega t \, d\omega t \right] \right]^{1/2}$$

$$= \left[\frac{V_m^2}{4\pi} \left((\omega t)_0^\pi - \left(\frac{\sin 2\omega t}{2} \right)_0^\pi \right) \right]^{1/2}$$

$$= \left[\frac{V_m^2}{4\pi} (\pi) - 0 \right]^{1/2}$$

$$V_{rms} = \frac{V_m}{2} \quad \dots \textcircled{7}$$

Substitute $\textcircled{3}$ & $\textcircled{7}$ in equ $\textcircled{2}$ we get.

$$\Gamma = \sqrt{\frac{V_m^2/4}{V_m^2/\pi^2} - 1} = \sqrt{\frac{\pi^2}{4} - 1} = 1.21 \parallel \dots \textcircled{8}$$

Only $\frac{I_m}{2}$ not $\frac{I_m}{\sqrt{2}}$

$$\therefore \text{TUF} = \frac{\frac{I_m^2 R_L}{\pi^2}}{\frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{2}} = \frac{\frac{V_m^2}{\pi^2 R_L}}{\frac{V_m}{\sqrt{2}} \cdot \frac{V_m}{2 R_L}} = \frac{2\sqrt{2}}{\pi^2} = 0.287$$

Form factor:-

$$\begin{aligned} \text{Form factor} &= \frac{\text{rms value}}{\text{average value}} \\ &= \frac{V_m/2}{V_m/\pi} = \frac{\pi}{2} = 1.57 \end{aligned}$$

Peak factor:-

$$\begin{aligned} \text{Peak factor} &= \frac{\text{Peak value}}{\text{rms value}} \\ &= \frac{V_m}{V_m/2} = 2 \text{ II.} \end{aligned}$$

Problem:-

A voltage of $200 \cos \omega t$ is applied to HWR with load resistance of $5k\Omega$. Find the maximum d.c current component, rms current, ripple factor, TUF and rectifier efficiency.

Given data:-

$$\text{Applied Voltage} = 200 \cos \omega t$$

$$\therefore V_m = 200 \text{ V} ; R_L = 5k\Omega$$

Sol:-

i) To find d.c current:

$$I_m = \frac{V_m}{R_L} = \frac{200}{5 \times 10^3} = 40 \text{ mA}$$

$$\text{w.r.t. } I_{dc} = \frac{I_m}{\pi} = \frac{40 \times 10^{-3}}{3.14} = 12.73 \text{ mA}$$

ii) To find rms current:

$$I_{rms} = \frac{I_m}{2} = \frac{40 \text{ mA}}{2} = 20 \text{ mA}$$

These are two types of full-wave rectifiers (i) Full wave rectifier with center tapped transformer (ii) Full-wave rectifier without center tapped transformer (Bridge rectifier)

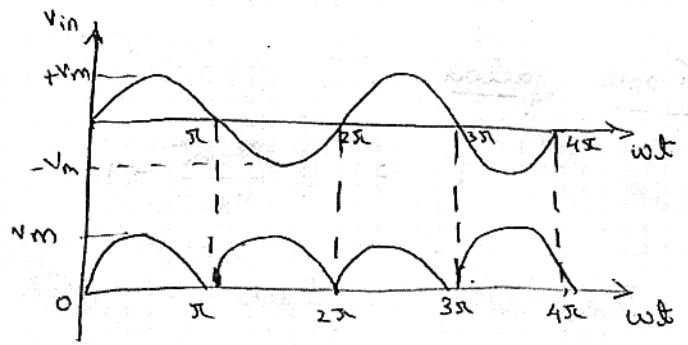
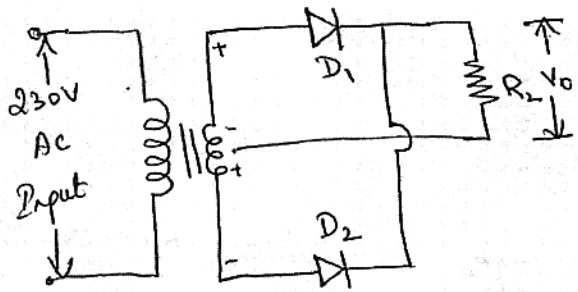


fig. Full wave rectifier with center tapped transformer.

When the transformer output voltage is positive at top as illustrated in fig. the anode of D_1 is positive and the center tap of the transformer is connected to the cathode of D_1 via R_L . Consequently, D_1 is forward biased and load current (I_L) flows from the top of the transformer secondary through D_1 through R_L from top to bottom and back to the transformer center tap. During this time the polarity of the voltage from the bottom half of the transformer secondary causes diode D_2 to be reverse biased.

For the duration of the negative half cycle of the transformer output, the polarity of the transformer secondary voltage causes D_1 to be reverse biased and D_2 to be forward biased. I_L flows from the bottom terminal of the transformer secondary through diode D_2 through R_L from top to bottom and back to the

RMS value of the voltage at the load resistance is

$$\begin{aligned}
 V_{rms} &= \left[\frac{1}{2\pi} \int_0^{2\pi} V_m^2 \sin^2 \omega t \, d(\omega t) \right]^{1/2} \\
 &= \left[\frac{V_m^2}{2\pi} \int_0^\pi \sin^2 \omega t \, d(\omega t) \right]^{1/2} \quad \sin^2 \theta = \frac{1 - \cos 2\theta}{2} \\
 &= \left[\frac{V_m^2}{\pi} \int_0^\pi \sin^2 \omega t \, d(\omega t) \right]^{1/2} = \left[\frac{V_m^2}{\pi} \int_0^\pi \frac{(1 - \cos 2\omega t)}{2} \, d(\omega t) \right]^{1/2} \\
 &= \left[\frac{V_m^2}{2\pi} \left(\int_0^\pi d(\omega t) - \int_0^\pi \cos 2\omega t \, d\omega t \right) \right]^{1/2} \\
 &= \left[\frac{V_m^2}{2\pi} \left((\pi - 0) - \left(\frac{\sin 2\omega t}{2} \right)_0^\pi \right) \right]^{1/2} \\
 V_{rms} &= \left[\frac{V_m^2}{2\pi} (\pi) \right]^{1/2} = \frac{V_m}{\sqrt{2}} \parallel
 \end{aligned}$$

$$\begin{aligned}
 \therefore \text{Ripple factor} &= \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1} \\
 &= \sqrt{\frac{(V_m/\sqrt{2})^2}{(2V_m/\pi)^2} - 1} = \sqrt{\frac{\pi^2}{2 \times 4} - 1}
 \end{aligned}$$

$$r = \sqrt{\frac{\pi^2}{8} - 1} = 0.482 \parallel$$

Efficiency:-

$$\begin{aligned}
 \eta &= \frac{\text{dc output power}}{\text{dc input power}} = \frac{P_{dc}}{P_{ac}} \\
 &= \frac{(V_{dc})^2/R_L}{(V_{rms})^2/R_L} = \frac{4V_m^2/\pi^2}{V_m^2/2} = \frac{8}{\pi^2} = 0.812 = 81.2\%
 \end{aligned}$$

because the entire secondary voltage appear across the (18)
non-conducting diode.

Problem:-

A 230V, 60Hz voltage is applied to the primary of a 5:1 step down center tap transformer use in a full wave rectifier having a load of 900Ω . If the diode resistance and secondary coil resistance together has a resistance of 100Ω determine (a) d.c. voltage across the load (b) d.c current flowing through the load (c) d.c power delivered to the load (d) PIV across each diode (e) ripple voltage and its frequency (f) rectification efficiency.

Given data:-

$$\text{Input signal} = 230\text{V}, 60\text{Hz}$$

$$\text{step down transformer} = 5:1$$

$$R_L = 900\Omega$$

$$r_f + r_s = 100\Omega$$

Sol:-

$$\text{The voltage across the two ends of secondary} = \frac{230}{5} = 46\text{V}$$

$$\text{Voltage from center tapping to one end } V_{rms} = \frac{46}{2} = 23\text{V}$$

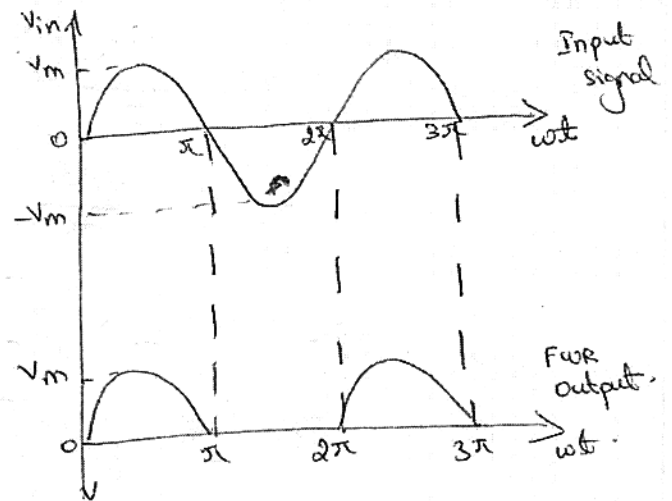
$$(a) \quad V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 23 \times \sqrt{2}}{3.14} = 20.7\text{V}$$

$$(b) \quad I_{dc} = \frac{V_{dc}}{(r_s + r_f + R_L)} = \frac{20.7}{[100 + 900]} = 20.7\text{mA}$$

$$(c) \quad \text{Dc power delivered to load } P_{dc} = I_{dc}^2 R_L = (20.7\text{mA})^2 (900)$$

$$P_{dc} = 0.386\text{W}$$

diodes D_1 and D_3 do not conduct. The conducting diode D_2 and D_4 will be in series through the load R_L and the current flows through R_L in the same direction as in the previous half cycle. Thus the bidirectional wave is converted into a unidirectional.



Ripple factor (Γ) :-

$$\Gamma = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1}$$

The average voltage (or) dc voltage available across the load resistance is

$$\begin{aligned} V_{dc} &= \frac{1}{2\pi} \int_0^{2\pi} V_m \sin \omega t \, d(\omega t) \\ &= \frac{1}{2\pi} \left[\int_0^{\pi} V_m \sin \omega t \, d(\omega t) \right] \\ &= \frac{V_m}{\pi} \left[-\cos \omega t \right]_0^{\pi} = \frac{-V_m}{\pi} [-1 - 1] \end{aligned}$$

$$V_{dc} = \frac{2V_m}{\pi} \quad ||.$$

$$V_{rms} = \left[\frac{V_m^2}{2\pi} \left\{ (\pi-0) - (0) \right\} \right]^{1/2}$$

$$= \left[\frac{V_m^2}{2\pi} (\pi) \right]^{1/2}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$\therefore \text{Ripple factor} = \sqrt{\frac{V_{rms}^2}{(V_{dc})^2} - 1}$$

$$= \sqrt{\frac{(V_m/\sqrt{2})^2}{(2V_m/\pi)^2} - 1} = \sqrt{\frac{\pi^2}{8} - 1}$$

$$\text{Ripple factor } (r) = 0.482$$

Efficiency:

$$\eta = \frac{\text{dc output power}}{\text{dc input power}} = \frac{P_{dc}}{P_{ac}}$$

$$\eta = \frac{(V_{dc})^2 / R_L}{(V_{rms})^2 / R_L} = \frac{(2V_m/\pi)^2}{(V_m/\sqrt{2})^2} = \frac{8}{\pi^2}$$

$$\eta = 0.812 \text{ (or) } 81.2 \%$$

Transformer utilization factor (TUF):

The TUF of the full wave bridge rectifier is obtained by

$$TUF = \frac{\text{dc power, delivered to the load}}{\text{ac rating of the transformer secondary}}$$

For full wave bridge rectifier circuit the rated voltage of the transformer secondary is $V_m/\sqrt{2}$ and the rms current flowing through the winding is $I_m/\sqrt{2}$

Comparison of different rectifiers

S.No.	Particulars	Half Wave Rectifier.	Full Wave Rectifier.	Bridge Rectifier.
1.	No of diodes	1	2	4
2.	Maximum efficiency	40.6 %	81.2 %	81.2 %
3.	V_{dc} (no load)	V_m / π	$2V_m / \pi$	$2V_m / \pi$
4.	V_{rms}	$V_m / 2$	$V_m / \sqrt{2}$	$V_m / \sqrt{2}$
5.	Ripple factor	1.81	0.48	0.48
6.	Peak inverse voltage	V_m	$2V_m$	V_m
7.	Transformer utilisation factor	0.287	0.693	0.812
8.	Form factor	1.57	1.11	1.11
9.	Peak factor	2	$\sqrt{2}$	$\sqrt{2}$
10.	Output frequency	f	$2f$	$2f$
11.	Average current	I_{dc}	$I_{dc} / 2$	$I_{dc} / 2$

The metal film anode connection is patterned to allow most of the light to be emitted. A gold film is applied to the bottom of the substrate to reflect as much light as possible towards the surface of the device and to provide a cathode connection. Using various materials LED can be manufactured to produce light of virtually any color.

- GaAs - Emit infrared (invisible) radiation
- GaAsP - Emit red or yellow light.
- GaP - Emit red or green light.

Construction:-

The typical construction of LED is shown in fig (b). The pn junction is mounted on a cup shaped reflector, wires are provided for anode and cathode connection and the device is encapsulated in an epoxy lens. The lens can be clear or colored and the lens color identifies the LED light color. In some LEDs have glass particles embedded in the epoxy lens to diffuse the emitted light and increase the viewing angle of the device. The LED circuit symbol is shown in fig (c). The arrow directions in the symbol indicate emitted light.

Characteristics and Parameters:-

LED characteristics are similar to those of other semiconductor diodes, except that the typical forward

Advantages of LED:-

1. LEDs are small in size therefore thousand LEDs can be packed in one sq. metre area.
2. The brightness of light emitted by LED depends on the current flowing through LED. So brightness of light can be smoothly controlled by varying the current.

Disadvantages of LED:-

1. Luminous efficiency of LED is low which is about 1.5 lumens/watt
2. Need large power for the operation compared to normal P-n junction diode.

Applications:-

1. All kinds of visual display (eg) Seven Segment display and alpha numeric displays. Such displays are commonly used in watches and calculators.
2. Some LED radiate infrared light which is invisible and used in remote control and application like burglar alarm.

LASER DIODE:-

The term laser stands for light amplification by stimulated emission of radiation.

Laser light is referred to as coherent light which means that a light with a single wavelength.

reflected back again from the other end of the junction.

This movement of photons from one end to another and continues for thousands time. During this movement, photons strike more atoms and release additional photons due to the avalanche effect.

This activity of reflection and generation of increasing number of photons results in a very intense focused and pure beam of laser light which is formed by the photons that pass through the partially reflective end of pn junction.

Each photons produced in such an emission process is identical to the other photons in energy level and frequency. Thus emission process gives a intense beam of laser light with a single wavelength.

Application:

1. Used in CD players and optical discs
2. Laser printers
3. Fiber and broadband Communication.

Zener diode:

The zener diode is, a silicon p-n junction Semiconductor device, which is generally operates in its reverse breakdown region. The zener diodes are fabricated with precise breakdown voltage by controlling the doping level during manufacturing. The zener diode has breakdown

Collision, the valence electron in covalent bond becomes free and accelerate. This further collides with another valence electron to make it free. This is called carrier multiplication. This action is very fast to generate large electron-hole pairs and breakdown occurs which is called zener & avalanche breakdown.

Characteristic of zener diode:

In the forward biased condition the normal rectifier diode and the zener diode operate in similar fashion, but the zener diode is designed to be operated in the reverse biased condition. In reverse biased condition the diode carries reverse saturation current till the reverse voltage applied is less than the reverse breakdown voltage.

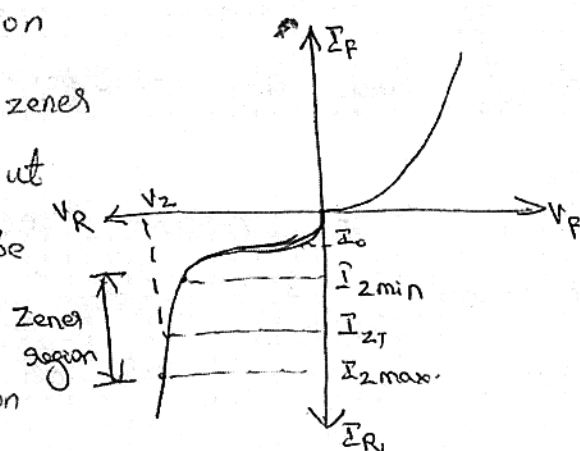


Fig. V-I characteristics of zener diode.

When the reverse voltage exceeds reverse breakdown voltage, the current through it changes drastically but the voltage across it remains almost constant. Such a breakdown region is a normal operating region of a zener diode. Such a sharp change in the reverse characteristic is called knee (or) zener knee. The reverse bias voltage at which the breakdown occurs is called zener breakdown voltage, denoted as V_Z .

Resistance Z_Z .

$$Z_Z = \frac{\Delta V_Z}{\Delta I_Z} = \frac{1}{\left(\frac{\Delta I_Z}{\Delta V_Z}\right)} = \left[\text{slope of the reverse characteristic in zener region} \right]$$

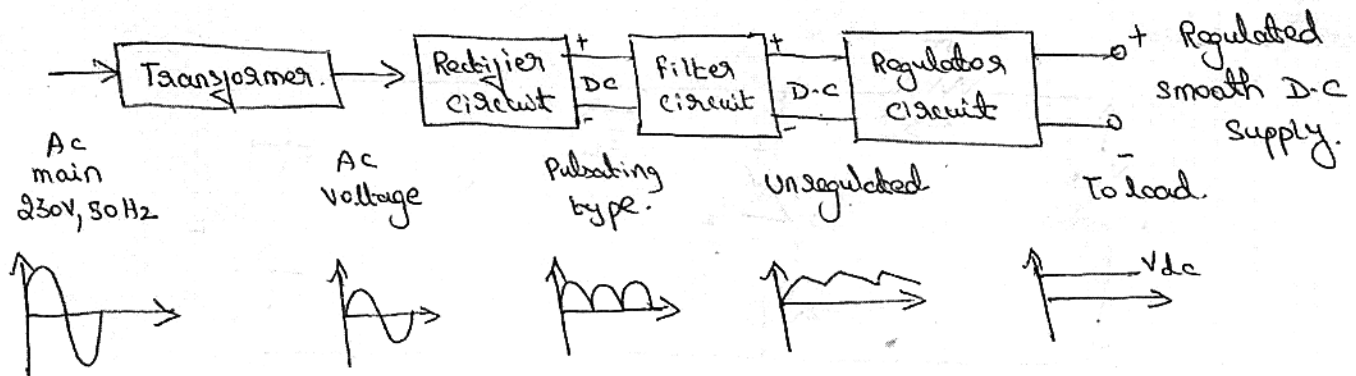
Application of Zener Diode:

The various applications of zener diode are

1. As a voltage regulating element in voltage regulators.
2. In various protection circuits.
3. In clipping circuits it is used to clip off the unwanted portion of the voltage waveform.

Block Schematic of regulated power Supply:

A typical d.c. power supply consists of various stages. The block diagram of d.c. power supply is shown below.



The ac voltage is connected to the primary of the transformer. The transformer step down the ac voltage to the level required for the desired dc output.

The rectifier circuit converts this ac voltage into a pulsating dc voltage. A pulsating dc voltage

is equal to the zener voltage V_Z . Thus the Zener diode acts as an ideal voltage source which maintains a constant load voltage independent of the current.

Regulation with Varying Input Voltage.

The zener regulator under varying input voltage condition is shown below.

$$V_o = V_Z \quad \dots (1)$$

$$I = I_Z + I_L \quad \dots (2)$$

$$\text{where } I_L = \frac{V_Z}{R_L} \quad \dots (3)$$

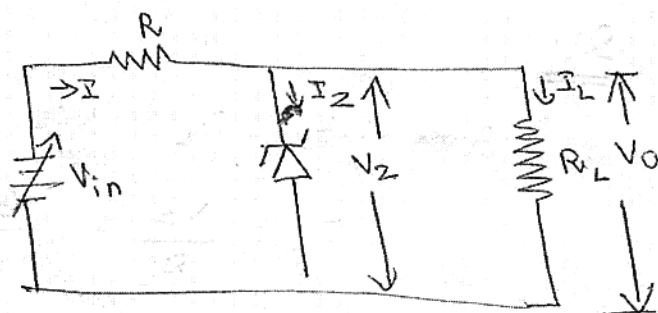


Fig. Varying input condition

Now if V_{in} increases, then the total current I increases. But I_L is constant as V_Z is constant. Hence the current I_Z increases to keep I_L constant.

But as long as I_Z is between I_{Zmin} and I_{Zmax} the o/p voltage is constant.

Similarly if V_{in} decreases then current I decreases. But to keep I_L constant I_Z decreases. As long as I_Z is between I_{Zmax} and I_{Zmin} , the output voltage remains constant.

The maximum power dissipation for the zener diode is fixed and given by.

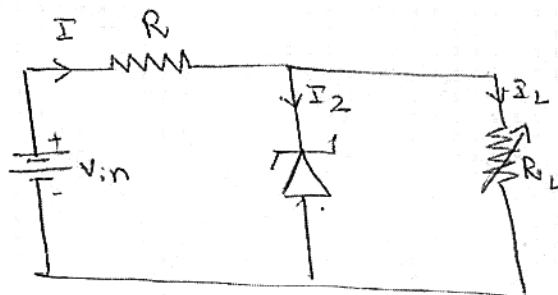
$$P_D = V_Z I_{Zmax}$$

Regulation with Varying Input Voltage.

28

The zener regulator under varying load condition and constant input voltage is shown below.

The input voltage is constant while the load resistance R_L is variable. As V_{in} is constant and $V_o = V_Z$



$$\therefore V_{in} = IR + V_Z$$

$$\text{where } I = I_Z + I_L$$

If R_L decreases then I_L increases, to keep I constant I_Z should be decrease but as long as it is between I_{Zmin} and I_{Zmax} output voltage V_o will be constant.

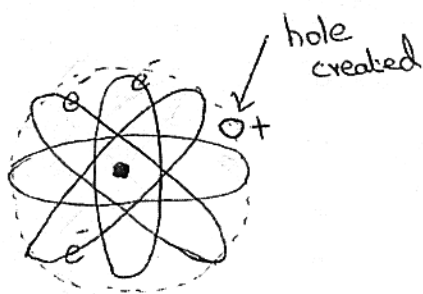
Similarly if R_L increases then I_L decreases, to keep " I " constant, I_Z increases. but as long as it is between I_{Zmin} and I_{Zmax} output voltage V_o will be constant.

of two types of particles, protons and neutrons. Protons have a positive electrical charge, equal in magnitude to (but, opposite in polarity) to the negative charge on an electron. A neutron has no charge at all.

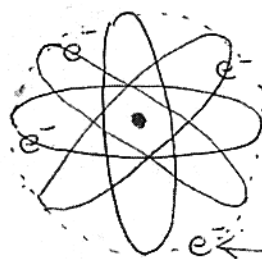
Protons and neutrons each have masses about 1800 times the mass of an electron. For a given atom, the number of protons in the nucleus normally equals the number of orbiting electrons.

Since the protons and orbital electrons are equal in number and equal and opposite in charge, they neutralise each other electrically. For this reason, all atoms are normally electrically neutral.

If an atom loses an electron, it has lost some negative charge. Thus it becomes positively charged and is referred to as a positive ion. Similarly if an atom gains an additional electron, it becomes negatively charged and is termed as negative ion.



(a) Positive Ion



(b) Negative Ion

The number of protons in an atom is referred to as the atomic number of the atom.

electron in a shell where one could exist.

The closer an electron is to the nucleus, the stronger are the forces that bind it. Each shell has an energy level associated with it that represents the amount of energy required to extract an electron from the atom. Since the electrons in the valence shell are farthest from the nucleus, they require the least amount of energy to extract them.

Conversely those electrons closest to the nucleus require the greatest energy application to extract them from the atom. The energy levels of the orbiting electrons are measured in electron volts (eV). An electron volt is defined as the amount of energy required to move one electron through a voltage difference of one volt.

Energy Band:-

In any given material there are two distinct energy bands in which electrons may exist, the valence band and the conduction band. Separating these two bands is an energy gap, termed the forbidden gap in which no electrons can normally exist. The valence band, conduction band and forbidden are shown in fig.

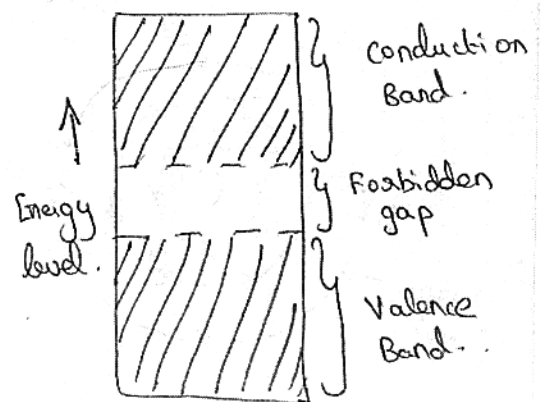


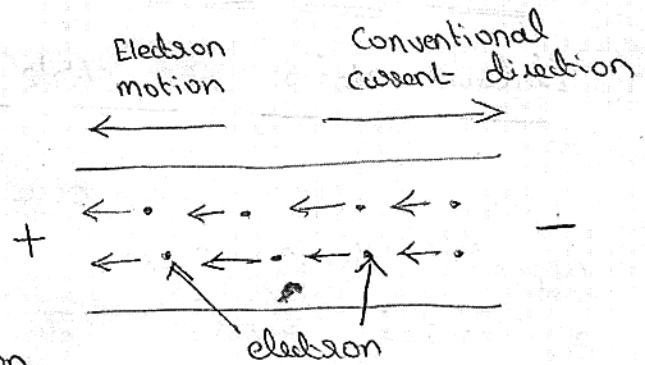
fig. Energy Band Diagram.

Electrons within the conduction band have become disconnected from atoms and are drifting around within the material. Conduction band electrons may be

energy to enable it to escape from its atom. Free electrons require less application of energy than holes to move them because they are already disconnected from their atoms. For this reason, electrons have greater mobility than holes.

Current flow from positive to negative is referred to as the conventional current direction.

Electron flow from negative to positive is known as the direction of electron flow.



Conductors:

Whether a material is a conductor, semiconductor or an insulator depends largely upon what happens to the outer shell electrons when the atoms bond themselves together to form a solid.

In case of conductors (e.g. copper) the easily detached valence electrons are given up by the atoms. This will create a great mass of free electrons drifting about in the space between the copper atoms.

The electrons are easily moved under the influence of an applied voltage to create a current flow. The bonding force that holds atoms together in a conductor is known as metallic bonding.

n-Type and p-Type Semiconductors:

Doping:

Pure Semiconductor material is known as intrinsic material. Before intrinsic material can be used for device manufacture, impurity atoms must be added to improve its conductivity. The process of adding the atom is termed doping. Two different types of doping are possible namely donor doping and acceptor doping.

The donor doping generates free electrons in the conduction band and acceptor doping produces valence band holes or a shortage of valence electrons in the material. After doping the semiconductor is known as extrinsic material.

N-Type MATERIAL:

In donor doping the pentavalent atom is added to the undoped material. The impurity atoms form covalent bonds with the silicon or germanium atom because the semiconductor atoms have only four electrons in their valence shells, there is one extra valence shell electron for each impurity atom added. Each ~~electron~~ additional electron produced in this way enters the conduction band as a free electron. It is shown in below fig where there is no hole for the fifth electron from the outer shell of the impurity atom therefore this electron

becomes a free electron because the free electrons have negative charges, donor-doped semiconductor is known as n-type material. Typical donor materials are antimony, phosphorus and arsenic. Since these atoms have five valence electrons, they are referred to as pentavalent atoms.

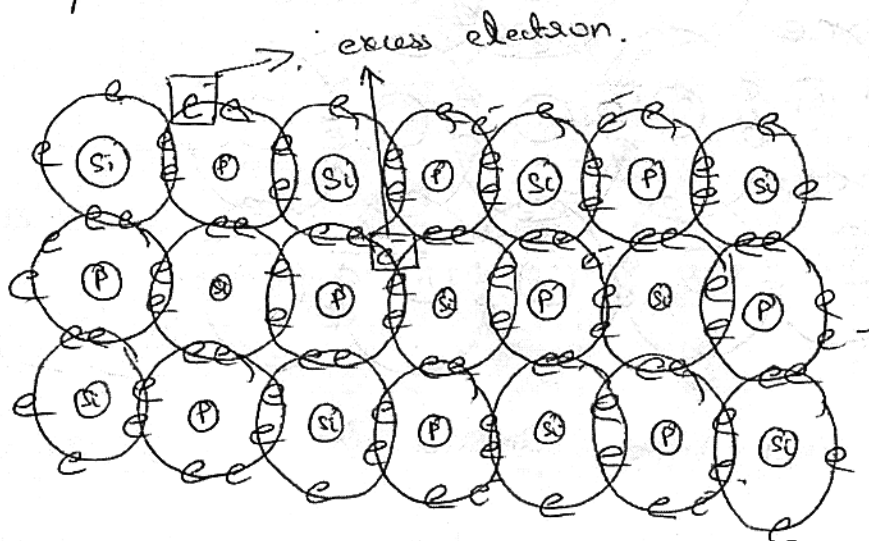


fig. N-type semiconductor.

P-type Material:

In acceptor doping trivalent atoms is added to the undoped material. These atoms form covalent bonds with the semiconductor atoms but the bonds lack one electron for a complete outer shell of eight. Therefore an impurity atom has only three valence electrons, a hole exists in the bond with the surrounding atoms. So here conduction may occur by the process of hole transfer.

have negative temperature coefficient.

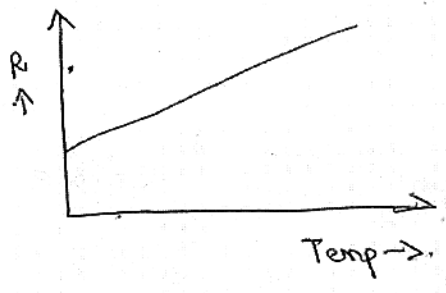


Fig. Conductor has positive temperature coefficient.

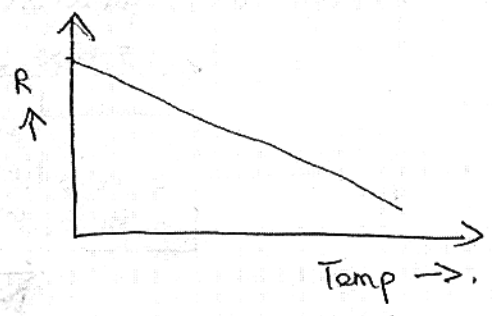


Fig. Semiconductor has negative temperature coefficient.

PN JUNCTION DIODE:-

The term diode identifies a two electrode or two terminal device. A semiconductor diode is simply a pn junction with a connecting lead on each side. A diode is a one way device offering a low resistance when forward biased and behave almost as an open switch when reversed biased.

The circuit symbol for a diode is an arrowhead and bar. The arrowhead indicates the conventional direction of current flow when diode is forward biased.

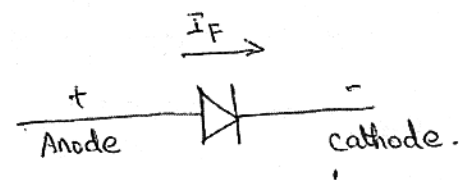


Fig. diode under forward biased condition.

PN Junction Formation:-

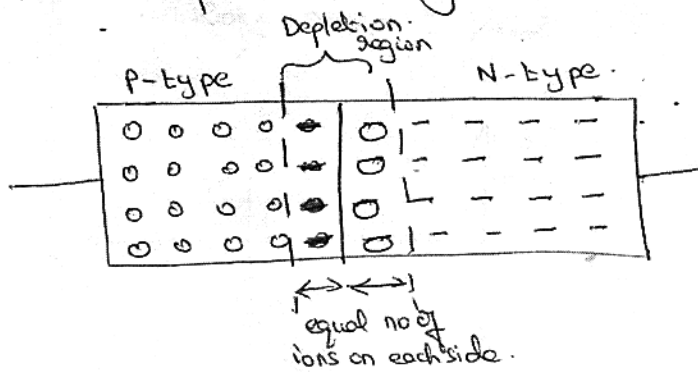
PN junction diode consists of two blocks of semiconductor where one block is p-type material and other block is n-type material. The p-type and n-type

voltage at 25°C are 0.3V for germanium junction ⑦
and 0.7V for silicon.

Depletion region:-

The movement of charge carriers across the junction leaves a layer on each side which is depleted of charge carriers. This is called depletion region. On the n-side the depletion region consists of donor impurity atom which, having lost the free electron associated with them, have become positively charged. Similarly on p-side is made up of acceptor impurity atoms which have become negatively charged by losing the holes associated with them.

On each side of the junction, equal number of impurity atoms are involved in depletion region. If two blocks of semiconductor material have equal doping densities, the depletion layer on each side have equal widths.



Forward and Reverse biased Characteristics of PN junction diode:-

Forward Biased :-

When an external bias voltage is applied to a pn-junction, positive to the p-side and negative to the

on the junction area, temperature and semiconductor materials.

The characteristics of a germanium diode are similar to those of a silicon diode with some important difference. The forward voltage drop of a germanium device is typically 0.3V compared to 0.7V for silicon. For a germanium device the reverse saturation current at 25°C may be around $1\mu\text{A}$, which is much larger than the reverse current for a silicon diode. Finally the reverse breakdown voltage for germanium device is likely to be substantially lower than that of silicon device. These characteristics makes silicon diode preferable to germanium devices for most application.

Dynamic resistance.

The dynamic resistance of the diode is the resistance offered to changing levels of forward voltage. The dynamic resistance also known as the incremental resistance (or) ac resistance is the reciprocal of the slope of the forward characteristics beyond the knee.

$$r_d = \frac{\Delta V_F}{\Delta I_F}$$

Static resistance:-

This is the forward resistance of p-n junction diode in forward biased when p-n junction

This combined effect of movement of the charge carriers constitutes a current known as the drift current. Thus the drift current is defined as the flow of electric current due to the motion of the charge carriers under the influence of an external electric field. The drift current density due to the charge carriers such as free electrons and holes are the current passing through a square centimeter perpendicular to the direction of flow.

The equation for the drift current density J_n due to free electron is given by

$$J_n = q n \mu_n E A / \text{cm}^2$$

Similarly the drift current density J_p due to holes is given as

$$J_p = q p \mu_p E A / \text{cm}^2$$

where,

n - no of free electrons per cubic centimetre

p - no of holes per cubic centimetre.

μ_n - mobility of electrons in $\text{cm}^2/\text{V-s}$

μ_p - mobility of holes in $\text{cm}^2/\text{V-s}$

E - Applied electric field intensity in V/cm

q : charge of an electron (coulomb)

Diffusion current :-

It is possible for an electron electric current to flow in a semiconductor even in the absence of the applied voltage provided a concentration gradient exists in the material. A concentration gradient exists if the no

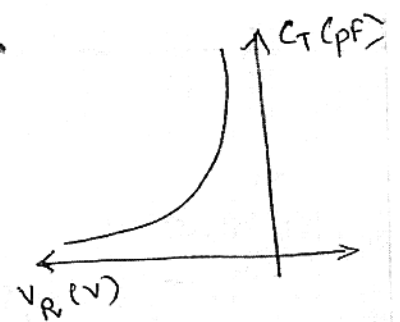
As the charged particles move away from the junction there exists a change in charge with respect to the applied reverse voltage. So change in charge dQ with respect to the change in voltage dV is nothing but a capacitive effect. This capacitance effect is called transition capacitance (C_T).

$$C_T = \frac{dQ}{dV}$$

If " W " is the width of the depletion region then the transition capacitance is given by.

$$C_T = \frac{\epsilon A}{W}$$

A - Area of cross section of the junction
 ϵ - Permittivity of the semiconductor.



As the reverse biased applied to the diode increases, the width of the depletion region increases. Thus the transition capacitance C_T decreases. As the transition capacitance varies with the applied voltage, it can be used as a voltage variable capacitance in many applications.

Diffusion Capacitance:-

In forward biased condition, the width of the depletion region decreases and holes from p-side get diffused in n-side while electrons from n-side move into p-side. As the applied voltage increases concentration of injected charged particles increases. This rate of change of the injected charge with applied voltage is defined as a capacitance called diffusion capacitance.

across and the density of minority carriers diminishes to zero at this junction. The current which flows, the reverse saturation current I_0 , is small because the density of thermally generated minority carriers is very small.

If the external voltage is suddenly reversed on a diode circuit which has been carrying current in the forward direction the diode current will not immediately fall to its steady state reverse voltage value. For the current cannot attain its steady state value until the minority carrier distribution which at the moment of voltage reversal had the form in fig a reduces to the distribution in fig b. Until such time as the injected minority carrier density $p_n - p_{n0}$ (or $n_p - n_{p0}$) has dropped normally to zero the diode will continue to conduct easily and the current will be determined by the external resistance in the diode circuit.

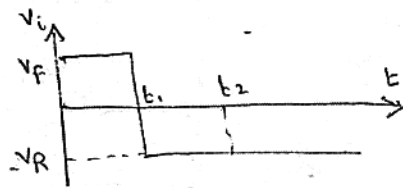
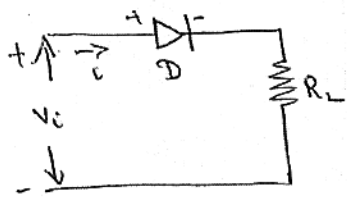


fig b voltage applied to diode circuit

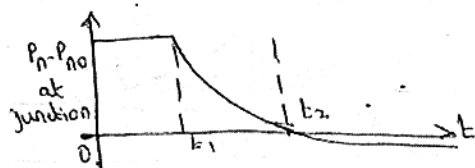


fig c The excess carrier density at the junction.

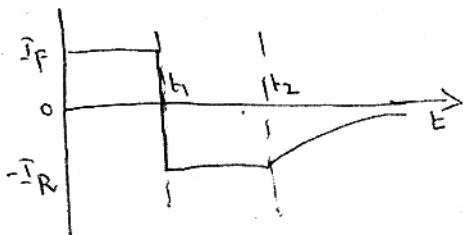


fig d. diode current

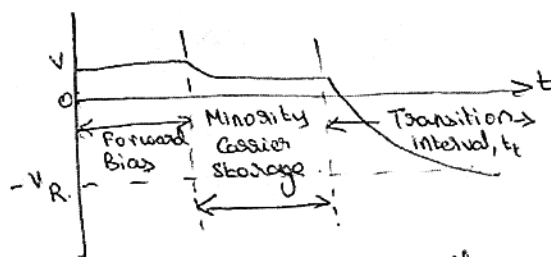


fig e. Diode voltage.

$$P_n(x) = P_n(0) e^{-x/L_p} \dots (6)$$

where L_p - diffusion length of holes
 x - distance from junction.

The diffusion hole current entering the n-side from p-side

$$I_{pn}(x) = -AeD_p \frac{d}{dx} [P_n(x)] \dots (7)$$

A - cross section area

D_p - Diffusion Constant

Now substitute equ (6) in (7) we get.

$$\begin{aligned} I_{pn}(x) &= -AeD_p \frac{d}{dx} [P_n(0) e^{-x/L_p}] \\ &= -AeD_p P_n(0) \frac{d}{dx} [e^{-x/L_p}] \\ &= -AeD_p P_n(0) e^{-x/L_p} \left(-\frac{1}{L_p}\right) \end{aligned}$$

$$I_{pn}(x) = \frac{AeD_p P_n(0)}{L_p} e^{-x/L_p} \dots (8)$$

The hole current at the junction i.e. $x=0$, equ (8) become

$$I_{pn}(0) = \frac{AeD_p P_n(0)}{L_p} = \frac{AeD_p p_{n0} (e^{V/V_T} - 1)}{L_p} \dots (9)$$

Similarly the electron current crossing the junction into the p-side at $x=0$ is.

$$I_{np}(0) = \frac{AeD_n n_{p0} (e^{V/V_T} - 1)}{L_n} \dots (10)$$

$\therefore$ The total diode current is

$$I = I_{pn}(0) + I_{np}(0) = I_0 (e^{V/V_T} - 1) \dots (11)$$

$$\text{where } I_0 = \frac{AeD_p p_{n0}}{L_p} + \frac{AeD_n n_{p0}}{L_n}$$

Rectifier:-

Rectifier is defined as an electronic device used for converting a.c voltage into unidirectional voltage. A rectifier utilizes unidirectional conduction devices like a vacuum diode or PN junction diode.

Rectifiers are classified depending upon the period of conduction as Half wave rectifier and full wave rectifier.

Half Wave Rectifier:-

It converts an a.c voltage into a pulsating d.c voltage using only one half of the applied a.c voltage. The below fig shows the basic circuit and waveform of a half wave rectifier.

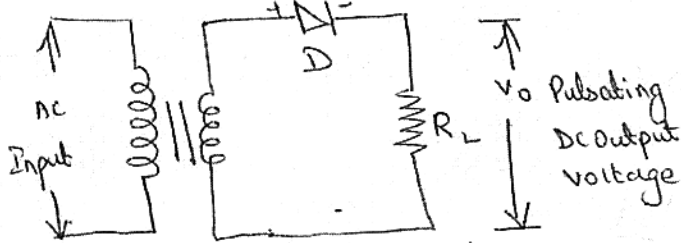


Fig. Basic structure of half wave rectifier.

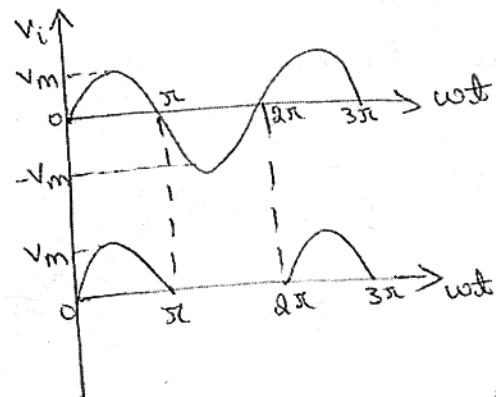


Fig. I/p - o/p waveform of half wave rectifier.

Let V_i be the voltage to the primary of the transformer and given by the equation.

$$V_i = V_m \sin \omega t ; \quad V_m \gg V_g$$

where V_g is the cut in voltage of the diode. During the positive half cycle of the input signal, the anode of the

$$\begin{aligned}
 V_{dc} &= \frac{1}{2\pi} \int_0^{2\pi} V_m \sin \omega t \, d(\omega t) \\
 &= \frac{1}{2\pi} \left[\int_0^{\pi} V_m \sin \omega t \, d(\omega t) + \int_{\pi}^{2\pi} 0 \cdot d(\omega t) \right] \\
 &= \frac{1}{2\pi} \int_0^{\pi} V_m \sin \omega t \, d(\omega t) \\
 &= \frac{V_m}{2\pi} \left[-\cos \omega t \right]_0^{\pi} = \frac{-V_m}{2\pi} [\cos(\pi) - \cos(0)] \\
 &= \frac{-V_m}{2\pi} [-1 - 1] = \frac{V_m}{\pi}
 \end{aligned}$$

$$V_{dc} = \frac{V_m}{\pi}$$

--- (3)

where $V = IR$

$\therefore$ replace LHS using ohms law

$$I_{dc} R_L = \frac{V_m}{\pi}$$

$$I_{dc} = \frac{V_m}{\pi R_L} = \frac{I_m R_L}{\pi R_L}$$

$$I_{dc} = \frac{I_m}{\pi} \quad \text{--- (4)}$$

If the value of diode forward resistance (r_f) and the transformer secondary winding resistance (r_s) are also taken into consideration then.

$$V_{dc} = \frac{V_m}{\pi} - [I_{dc} r_f + I_{dc} r_s]$$

$$V_{dc} = \frac{V_m}{\pi} - I_{dc} [r_f + r_s] \quad \text{--- (5)}$$

using ohms law

$$I_{dc} R_L = \frac{V_m}{\pi} - I_{dc} [r_f + r_s]$$

From the expression it is clear that the amount of a.c. present in the output is 12.1% of d.c. voltage.

Efficiency:-

The ratio of d.c. output power to a.c. input power is known as rectifier efficiency (η).

$$\eta = \frac{P_{d.c.}}{P_{a.c.}} = \frac{(V_{dc})^2 / R_L}{(V_{rms})^2 / R_L} = \frac{V_{dc}^2}{V_{ac}^2}$$

$$\eta = \frac{(V_m / \pi)^2}{(V_m / 2)^2} = \frac{4}{\pi^2} = 0.406 = 40.6\%$$

Peak Inverse Voltage (PIV):-

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. For half wave rectifier PIV is V_m .

Transformer Utilisation Factor (TUF)

In the design of any power supply the rating of the transformer should be determined.

$$TUF = \frac{\text{d.c. power delivered to the load}}{\text{a.c. rating of the transformer secondary}}$$

$$= \frac{P_{d.c.}}{P_{ac \text{ rated}}}$$

In half wave rectifying circuit the rated voltage of the transformer secondary is $V_m / \sqrt{2}$ but the actual rms current flowing through the winding is

c) Ripple factor:

$$\Gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{20 \times 10^{-3}}{12.73 \times 10^{-3}}\right)^2 - 1}$$

$$\Gamma = 1.21 //$$

d) To determine TUF:

$$TUF = \frac{P_{dc}}{P_{ac}(\text{rated})}$$

$$P_{dc} = I_{dc}^2 R_L = (12.73 \times 10^{-3})^2 \times 5 \times 10^3 = 0.81 \text{ W}$$

$$P_{ac}(\text{rated}) = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{2} = \frac{200}{\sqrt{2}} \times \frac{40 \times 10^{-3}}{2} = 2.828 \text{ W}$$

$$\therefore TUF = \frac{P_{dc}}{P_{ac}(\text{rated})} = \frac{0.81}{2.828} = 0.2863$$

e) Rectifier efficiency:

$$\eta = \frac{P_{dc}}{P_{ac}}$$

$$P_{ac} = I_{rms}^2 R_L = (20 \times 10^{-3})^2 \times 5 \times 10^3 = 2 \text{ W}$$

$$\therefore \eta = \frac{P_{dc}}{P_{ac}} \times 100 = \frac{0.81}{2} \times 100 = 40.5\%$$

Full Wave Rectifier:

It converts an a.c voltage into a pulsating d.c voltage using both half cycle of the applied a.c voltage. It uses two diodes of which one conducts during one half cycle while the other diode conducts during the other half cycle of the applied a.c voltage.

transformer center tap. The output wave is the combination of the two half cycles that is a continuous series of positive half cycles of sinusoidal waveform. This is full wave rectification.

Ripple factor:- (r)

$$r = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1}$$

The average voltage or dc voltage available across the load resistance is

$$\begin{aligned} V_{dc} &= \frac{1}{2\pi} \int_0^{2\pi} V_m \sin \omega t \, d(\omega t) \\ &= \frac{2}{2\pi} \int_0^{\pi} V_m \sin \omega t \, d(\omega t) \\ &= \frac{V_m}{\pi} \left[-\cos \omega t \right]_0^{\pi} = \frac{-V_m}{\pi} [-1 - 1] \end{aligned}$$

$$V_{dc} = \frac{2V_m}{\pi} //$$

If the diode forward resistance (r_f) and the transformer secondary winding resistance (r_s) are included in the analysis

$$V_{dc} = \frac{2V_m}{\pi} - [I_{dc} r_f + I_{dc} r_s]$$

$$I_{dc} R_L = \frac{2V_m}{\pi} - I_{dc} [r_f + r_s]$$

$$I_{dc} R_L + I_{dc} (r_f + r_s) = \frac{2V_m}{\pi}$$

$$I_{dc} [R_L + r_f + r_s] = \frac{2V_m}{\pi}$$

$$I_{dc} = \frac{2V_m}{\pi} \cdot \frac{1}{[R_L + r_f + r_s]} //$$

Transformer utilisation factor (TUF) :-

The average TUF in a full wave rectifying circuit is determined by considering the primary and secondary winding separately.

In the full wave rectifying circuit the rated voltage of the transformer secondary is $V_m/\sqrt{2}$ and rms current flow through the winding is $I_m/\sqrt{2}$.

$$\therefore TUF = \frac{P_{dc}}{P_{ac}(\text{rated})} = \frac{V_{dc}^2/R_L}{V_m/\sqrt{2} \cdot I_m/\sqrt{2}}$$
$$= \frac{4V_m^2/\pi^2 R_L}{V_m^2/2R_L} = \frac{8}{\pi^2} = 0.812$$

$$TUF \text{ for primary winding is } 2 [TUF \text{ of half wave rectifier}]$$
$$= 2 [0.287] = 0.574$$

$$TUF \text{ for full wave rectifier} = \frac{TUF \text{ of primary} + TUF \text{ of secondary}}{2}$$
$$= \frac{0.812 + 0.574}{2} = 0.693 \text{ ||}$$

Form factor :-

$$\text{Form factor} = \frac{\text{rms Value}}{\text{Avg Value}} = \frac{V_m/\sqrt{2}}{2V_m/\pi} = \frac{\pi}{2\sqrt{2}}$$

$$\text{Form factor} = 1.11$$

Peak factor :-

$$\text{Peak factor} = \frac{\text{Peak Value}}{\text{rms value}} = \frac{V_m}{V_m/\sqrt{2}} = \sqrt{2}$$

Peak inverse voltage for full wave rectifier is $2V_m$

d) PIV across each diode $PIV = 2V_m = 2 \cdot 23 \cdot \sqrt{2} = 65 \text{ V}$

e) ripple voltage $= \sqrt{(V_{rms})^2 - (V_{dc})^2}$
 $= \sqrt{(23)^2 - (20.1)^2} = 10.05 \text{ V}$

frequency of ripple factor $= 2 \times 60 = 120 \text{ Hz}$

f) efficiency $\eta = \frac{P_{dc}}{P_{ac}} = \frac{(V_{dc})^2 / R_L}{(V_{rms})^2 / R_L}$
 $= \frac{(20.1)^2}{(23)^2} = 0.81 = 81 \%$

Bridge Rectifier:

The need for a center tapped transformer in a full wave rectifier is eliminated in the bridge rectifier. As shown in fig in next page the bridge rectifier has four diodes connected to form a bridge. The a.c input voltage is applied to the diagonally opposite ends of the bridge. The load resistance is connected between the other two ends of the bridge.

For the positive half cycle of the input a.c voltage diode D_1 and D_3 conduct whereas diode D_2 & D_4 do not conduct. The conducting diodes will be in series through the load resistance R_L . So the load current is flows through R_L .

Similarly during negative half cycle of the input a.c voltage diode D_2 and D_4 conduct, whereas

where as using ohms law V_{dc} can be written as

$$I_{dc} R_L = \frac{2 I_m R_L}{\pi} \Rightarrow I_{dc} = \frac{2 I_m}{\pi}$$

If the diode forward resistance (r_f) and the transformer secondary winding resistance (r_s) are included in the analysis then.

$$V_{dc} = \frac{2 V_m}{\pi} - [I_{dc} r_f + I_{dc} r_s]$$

$$I_{dc} R_L = \frac{2 V_m}{\pi} - I_{dc} [r_f + r_s]$$

$$I_{dc} R_L + I_{dc} [r_f + r_s] = \frac{2 V_m}{\pi}$$

$$I_{dc} [R_L + r_f + r_s] = \frac{2 V_m}{\pi}$$

$$\therefore I_{dc} = \frac{2 V_m}{\pi} \frac{1}{[R_L + r_f + r_s]}$$

The r.m.s of the voltage at the load resistance is

$$V_{rms} = \left[\frac{1}{2\pi} \int_0^{2\pi} V_m^2 \sin^2 \omega t \, d(\omega t) \right]^{1/2}$$

$$= \left[\frac{V_m^2}{2\pi} \int_0^{2\pi} \sin^2 \omega t \, d(\omega t) \right]^{1/2} \quad \text{w.r.t. } \sin^2 \theta = \frac{1 - \cos 2\theta}{2}$$

$$\therefore V_{rms} = \left[\frac{V_m^2}{2\pi} \int_0^{2\pi} \left[\frac{1 - \cos 2\omega t}{2} \right] d(\omega t) \right]^{1/2}$$

$$= \left[\frac{V_m^2}{2\pi} \left\{ \int_0^{2\pi} d(\omega t) - \int_0^{2\pi} \cos 2\omega t \, d(\omega t) \right\} \right]^{1/2}$$

$$= \left[\frac{V_m^2}{2\pi} \left\{ (\omega t)_0^{2\pi} - \left(\frac{\sin 2\omega t}{2} \right)_0^{2\pi} \right\} \right]^{1/2}$$

$$\therefore \text{TVF} = \frac{P_{dc}}{P_{ac}(\text{rated})} = \frac{V_{dc}^2 / R_L}{V_m / \sqrt{2} \cdot I_m / \sqrt{2}}$$

$$\text{TVF} = \frac{(2V_m / \pi)^2 / R_L}{V_m / \sqrt{2} \cdot V_m / \sqrt{2} R_L} = \frac{8}{\pi^2} = 0.812 \text{ A.}$$

Form factor:

$$\text{Form factor} = \frac{\text{rms value}}{\text{Avg value}} = \frac{V_m / \sqrt{2}}{2V_m / \pi} = \frac{\pi}{2\sqrt{2}}$$

$$\text{Form factor} = 1.11$$

Peak factor: -

$$\text{Peak factor} = \frac{\text{Peak Value}}{\text{rms value}} = \frac{V_m}{V_m / \sqrt{2}} = \sqrt{2}$$

Peak inverse Voltage:

PIV for full wave bridge rectifier is V_m .

Advantages: -

1. No centre tap is required in the transformer secondary. Hence ac voltage can directly be applied to the bridge.
2. As two diodes conduct in series in each half cycle, inverse voltage appearing across diodes get shared. Hence the circuit can be used for high voltage application.

Disadvantages: -

The only disadvantage of bridge rectifier is it uses four diodes as compared to two diodes in normal full wave rectifier.

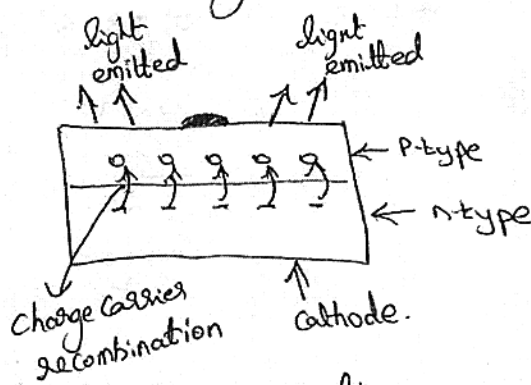
Application:

Used as rectifier in power circuits to convert ac to d.c.

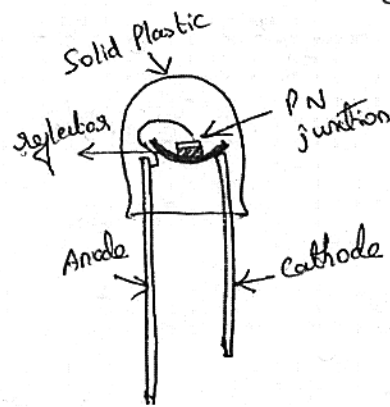
Light Emitting diode :- (LED)

charge carrier recombination occurs at a forward biased pn junction as electrons cross from the n-side and recombine with holes on the p-side. The free electrons have a higher energy level than holes on the p-side and some of the energy is dissipated in the form of heat and light when recombination takes place.

If the semiconductor material is translucent then light is emitted at the junction and the junction become light source. So it is called light emitting diode (LED).



(a) LED junction.



(b) LED Construction



(c) LED symbol

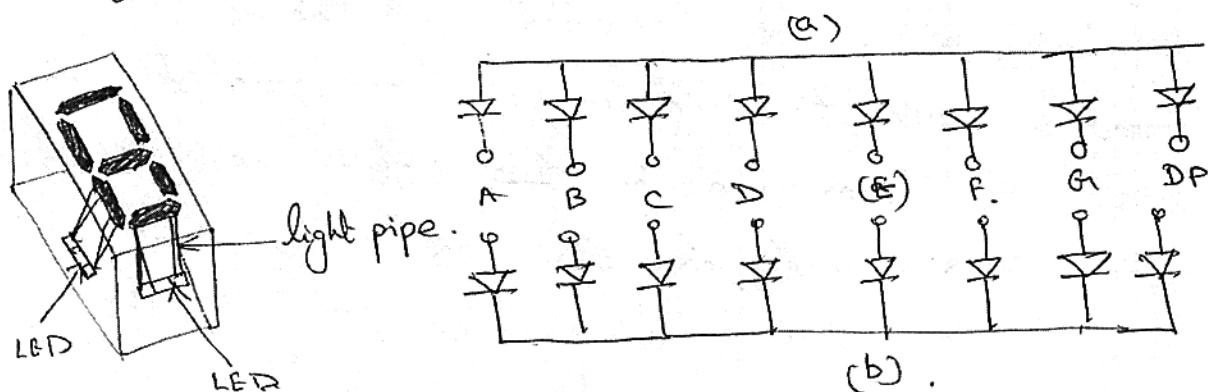
Working:

A cross sectional view of an LED junction is shown above fig. (a). The semiconductor material is gallium arsenide (GaAs), gallium phosphide (GaP) and gallium arsenide phosphide (GaAsP). An n-type epitaxial layer is grown upon a substrate and the p-region is created by diffusion. The charge carrier recombination occurs in the p-region so the p-region is kept uppermost to allow the light to escape.

drop is 1.6V, also the reverse breakdown voltage can be as low as 3V. The forward current used with a LED is usually in the 10mA to 20mA range but the peak current can be as high as 90mA. LED luminous intensity depends on the forward current level it is usually specified at 20mA. The peak wavelength

Seven Segment Display:-

The arrangement of a seven segment LED numerical display is shown below. The actual LED devices are very small. So to enlarge the lighted surface solid plastic light pipes are often used. Any desired numerical from 0 to 9 can be indicated by passing current through the appropriate segment.

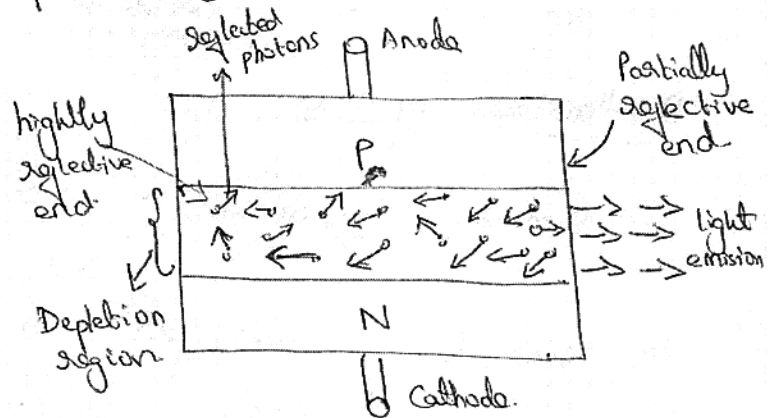
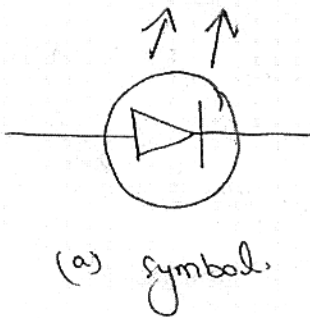


a) Common Anode Connection b) Common Cathode Connection.

The LEDs in a seven segment display may be connected in common anode (or) in common cathode configuration. When selecting the LED seven segment display it is important to determine which of the two connecting arrangements is required.

Construction:-

Laser consists of p-n junction formed by two doped gallium arsenide layers. The two ends of the structure are flat and parallel with one end mirrored and one partially reflective. The length (L) of the junction precisely related to the wavelength of the light to be emitted.

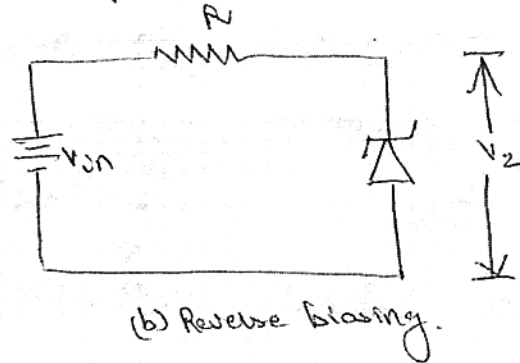
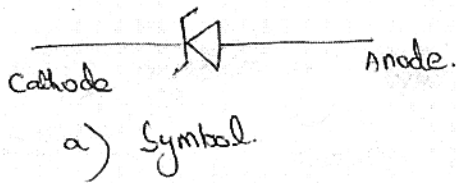


Working:-

When p-n junction is forward biased by an external voltage source, the electrons move through the junction and recombine as in an ordinary diode. When electrons recombine with holes, photons are released. These photons strike atom, causing more photons to be released.

As the forward bias current is increased, more electrons enter the depletion region and cause more photons to be emitted. Eventually some of the photons that are randomly drifting within the depletion region strike the reflective surface perpendicularly. So they are reflected back along their origin path. These reflected photons are then

voltage range from 3V to 200V. The d.c. voltage can be applied to the zener diode so as to make it forward biased or, reverse biased. The symbol of zener diode is shown below.



Breakdown Mechanisms in Zener diode:-

There are two distinct mechanisms due to which breakdown may occur in the zener diode. One is called zener breakdown and the other is avalanche breakdown.

1. Zener breakdown:-

When reverse bias voltage is less than 6V, there exists an intense electric field across the p-n junction. Due to this, high force is exerted on the valence electrons of atom, tending to separate them from respective nuclei. Hence electron-hole pairs are generated in large number and sudden increase of current is observed. This is called zener breakdown.

2. Avalanche Breakdown:-

When reverse voltage is greater than 6V the minority charge carrier accelerate. There are collisions between these carriers and electrons involved in the covalent bonds of the crystal. Due to this

The voltage V_Z is set by carefully controlling the doping level during manufacturing process.

The current corresponding to the knee point is called zener knee current and it is a minimum current zener must carry to operate on reverse breakdown region. It is denoted as I_{Zmin} .

The current at which the nominal zener breakdown voltage is specified is called zener test current, denoted as I_{ZT} , and the corresponding zener voltage is specified as V_Z .

As current increases, the power dissipation $P_Z = V_Z I_Z$ increase. If this dissipation increases beyond certain value, the diode may get damaged.

The maximum current a zener diode can carry safely is called zener maximum current and is denoted as I_{Zmax} . In practical circuit to limit the zener current between I_{Zmin} and I_{Zmax} a current limiting resistor is used in series with the zener diode.

The zener diode has Internal Resistance which is very small. In zener region this resistance is called dynamic resistance of the zener denoted as r_Z . However the zener region is not exactly vertical. The small change in zener current ΔI_Z produces a small change in zener voltage ΔV_Z . The ratio of ΔV_Z to ΔI_Z is called zener

means a unidirectional voltage containing large varying component called ripple on it.

The filter circuit used after the rectifier circuit which reduces the ripple content in the pulsating dc and tries to make it smoother.

A circuit used after the filter is a regulator circuit which not only makes the dc voltage smooth and almost ripple free. The output of the regulator is called dc supply to which the load can be connected.

Zener voltage regulator:-

The simplest shunt voltage regulator circuit uses a zener diode, to regulate the load voltage. The arrangement of zener diode in a regulator circuit is shown below

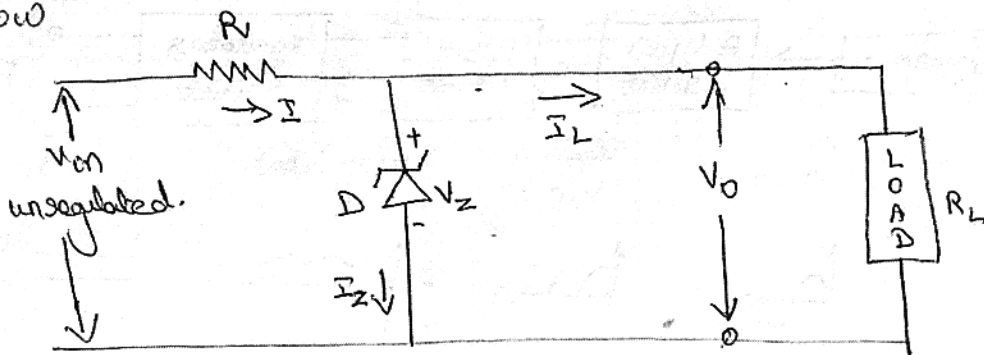
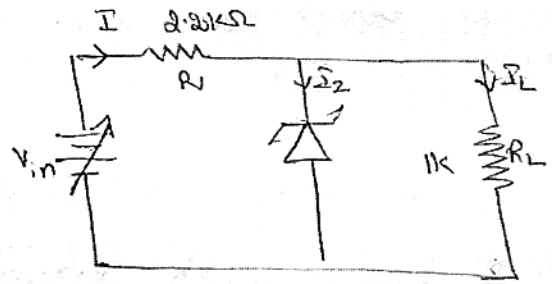


Fig. Zener diode as a shunt regulator.

After breakdown voltage, the voltage across the zener diode remains constant equal to its reverse bias condition which is equal to V_Z . This is connected across the load and hence the load voltage V_O is

Problem:-

For a zener regulator shown in fig. Calculate the range of input voltage for which output will remain constant.



$$V_Z = 6.1 \text{ V}, \quad I_{Z\min} = 2.5 \text{ mA}$$

$$I_{Z\max} = 25 \text{ mA}$$

Sol:-

$$\text{Given that } R_L = 1 \text{ k}\Omega, \quad V_Z = 6.1 \text{ V.}$$

$$\therefore I_L = \frac{V_Z}{R_L} = \frac{6.1}{1 \times 10^3} = 6.1 \text{ mA}$$

$$\text{For } V_{in(\min)}, \quad I = I_{Z\min} + I_L \\ = 2.5 \text{ mA} + 6.1 \text{ mA} = 8.6 \text{ mA}$$

$$\therefore V_{in(\min)} = V_Z + IR \\ = 6.1 + (8.6 \text{ mA})(2.2 \times 10^3) \\ = 25.02 \text{ V}$$

$$\text{For } V_{in(\max)}, \quad I = I_{Z\max} + I_L \\ = 25 \text{ mA} + 6.1 \text{ mA} = 31.1 \text{ mA}$$

$$\therefore V_{in(\max)} = V_Z + IR \\ = 6.1 + (31.1 \times 10^{-3})(2.2 \times 10^3)$$

$$V_{in(\max)} = 74.52 \text{ V}$$

Thus the range of input voltage is 25.02 V to 74.52 V.

UNIT II TRANSISTORS AND THYRISTORS

9

BJT, JFET, MOSFET- structure, operation, characteristics and Biasing UJT, Thyristors and IGBT - Structure and characteristics.

Unit-2

Bipolar Junction Transistor (BJT)

3

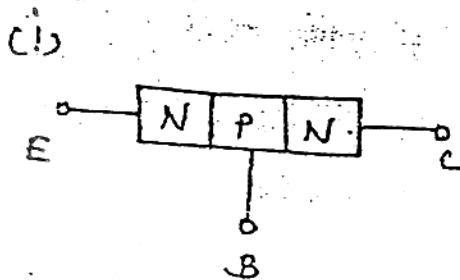
Construction

- Transistor consists of two PN junctions formed sandwiching either P type or n-type semiconductor between a pair of opposite types.

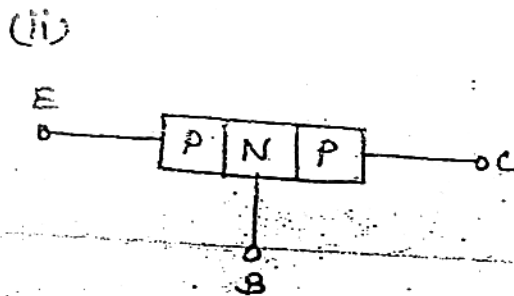
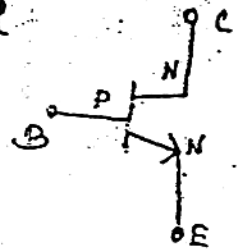
Types

(i) n-p-n Transistor

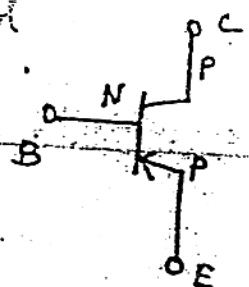
(ii) P-n-P Transistor



Symbol



Symbol



Three terminals

(i) Emitter (E)

(ii) Base (B)

(iii) Collector (C).

Emitter (E)

Region situated in one side of transistor, which supplies charge carriers, i.e., electrons or holes to other regions.

* heavily Doped region, moderate is

base (b)

Middle region that forms two PN junction in the transistor.

The base is very thin as compared to the emitter and is lightly doped region, small in size

Collector (c)

Region situated at the other side of the transistor, which collects charge carriers (i.e., electrons & holes).

The collector is always larger in size than base & emitter. & moderately doped

Dissipates heat.

The transistor has two junctions i.e. two diodes. (i) The junction between emitter and base may be called as emitter-base diode or emitter diode or emitter junction (J_E).

(ii) The junction between base and collector may be called as collector-base diode or collector diode or collector junction (J_C).

* emitter diode is always forward biased.

Resistance is small

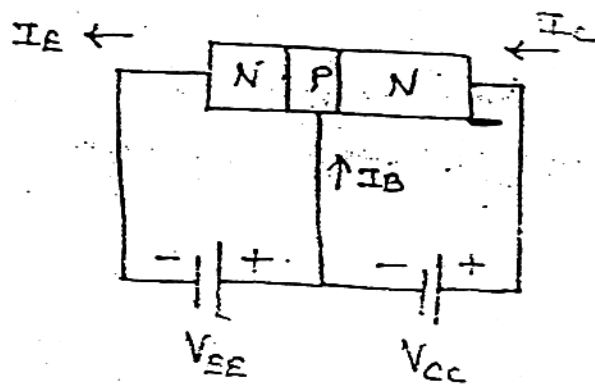
Forward bias applied is small

* Collector diode is always reverse biased

Resistance is large

Reverse bias applied on collector diode is larger.

1) Working of npn transistor



* emitter-base junction is forward biased

* Collector-base junction is reverse biased

The forward bias causes the electrons in the n-type emitter to flow through the p-type base, they combine with holes.

As the base is lightly doped & very thin, only a few electrons (5%) combine with holes, this forms base current I_B .

The remaining (95%) electrons recombine into the collector region to constitute collector current I_C .

$$I_E = I_B + I_C$$

Collector current consists of two components

1. majority carriers
2. minority carriers.

Minority current is called the leakage current I_{CBO} or I_{CO} .

$$\therefore I_C = I_{C \text{ majority}} + I_{C \text{ minority}}$$

I_C measured in milliamperes

I_{CO} measured in microamperes (μ) or nanoamperes

Types of Configuration

When a transistor is connected in a circuit, one terminal is used as an input terminal, the other terminal is used as an output terminal and the third terminal is common. (to Input + Output).

Depending upon the input, output + common terminal a transistor can be connected in three configurations

- (i) Common Base Configuration
- (ii) Common emitter Configuration
- (iii) Common collector Configuration

Common base Configuration

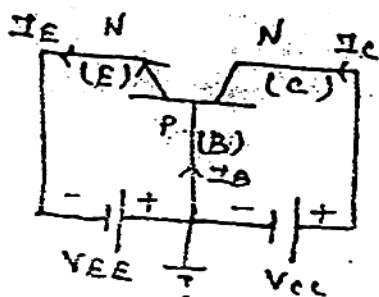
Also called as grounded base Configuration

In this Configuration

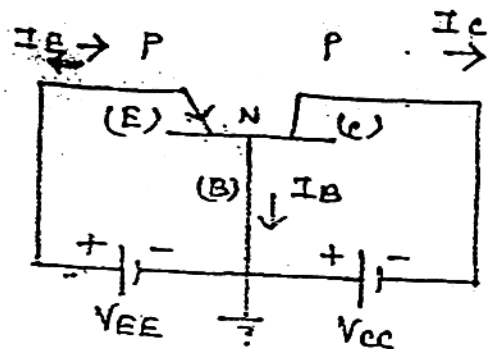
Emitter (E) is Input terminal

Collector (C) is output terminal

Base (B) is common terminal



NPN transistor



PNP transistor.

$$\therefore I_C = \alpha I_E + I_{\text{leakage}}$$

(a)

$$I_C = \alpha I_E + I_{CB0}$$

$$I_E = I_C + I_B$$

On substituting we get

$$I_C = \alpha (I_C + I_B) + I_{CB0}$$

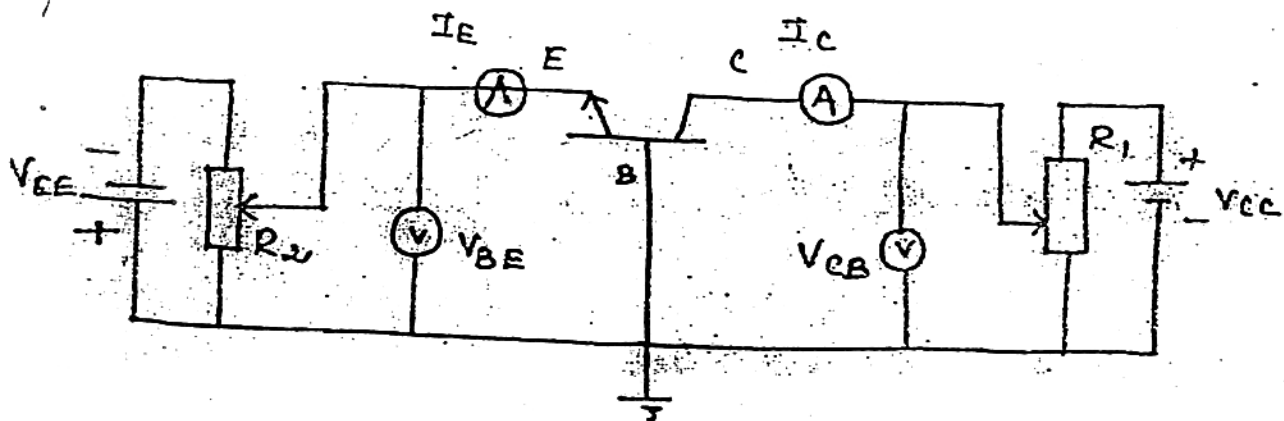
$$I_C = \alpha I_C + \alpha I_B + I_{CB0}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CB0}$$

$$I_C (1 - \alpha) = \alpha I_B + I_{CB0}$$

$$I_C = \frac{\alpha I_B}{1 - \alpha} + \frac{I_{CB0}}{1 - \alpha}$$

Common base circuit



Input characteristics

Relates Input emitter current I_E and input emitter base voltage V_{BE} at constant collector base output voltage V_{CB} .

input characteristics may be divided into three regions

1. Active region
2. Saturation region
3. Cut off region.

Active region

* Emitter Junction (J_E) forward biased, collector Junction (J_C) reverse biased.

* Collector collector current equals emitter current

$$I_C \approx I_E.$$

Saturation region

* Both emitter & collector junctions are forward biased

* Region left of $V_{CE} = 0$ & $I_E = 0$ in characteristics & the collector current I_C increases rapidly and becomes positive.

Cut off region

* Both emitter & collector junctions are reverse biased

* Current is very small in magnitude μA or nA .

* The region below $I_E = 0$ is known as cut-off region

ii) output admittance (h_{ob})

Ratio of Change in collector current to change in collector voltage with emitter current kept constant

$$h_{ob} = \frac{\Delta I_c}{\Delta V_{CB}} \bigg|_{I_E \text{ constant}}$$

Range 0.1 to 10 μmhos

i) Forward current gain (h_{fb})

Ratio of Change in collector current to change in emitter current with collector voltage kept constant

$$h_{fb} = \frac{\Delta I_c}{\Delta I_E} \bigg|_{V_{CB} \text{ constant}}$$

Range 0.9 to 1.0

iii) Reverse voltage gain (h_{rb})

Ratio of Change in emitter voltage to change in collector voltage with emitter current kept constant

$$h_{rb} = \frac{\Delta V_{BE}}{\Delta V_{CB}} \bigg|_{I_E \text{ constant}}$$

Range 10^{-5} to 10^{-4}

each value of I_E . This is repeated for different fixed values of I_E . Now the curves of I_C versus V_{CB} are plotted for constant values of I_E and the output characteristics thus obtained is shown in Fig. 6.9.

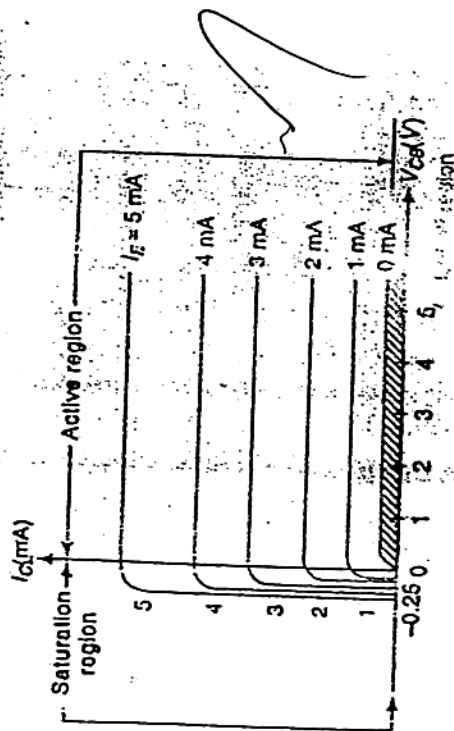


Fig. 6.9 CB output characteristics

From the characteristics, it is seen that for a constant value of I_E , I_C is independent of V_{CB} and the curves are parallel to the axis of V_{CB} . Further, I_C flows even when V_{CB} is equal to zero. As the emitter-base junction is forward biased, the majority carriers, i.e. electrons, from the emitter are injected into the base region. Due to the action of the internal potential barrier at the reverse biased collector-base junction, they flow to the collector region and give rise to I_C even when V_{CB} is equal to zero.

Early effect or base-width modulation As the collector voltage V_{CB} is made to increase the reverse bias, the space charge width between collector and base tends to increase, with the result that the effective width of the base decreases. This dependency of base-width on collector-to-emitter voltage is known as the *Early effect*. This decrease in effective base-width has three consequences:

- There is less chance for recombination within the base region. Hence, α increases with increasing V_{CB} .
- The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the emitter junction increases.
- For extremely large voltages, the effective base-width may be reduced to zero, causing voltage breakdown in the transistor. This phenomenon is called the *punch through*.

For higher values of V_{CB} , due to Early effect, the value of α increases. For example, α changes, say from 0.98 to 0.985. Hence, there is a very small positive slope in the CB output characteristics and hence the output resistance is not zero.

Transistor parameters The slope of the CB characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common base *hybrid parameters* or *h-parameters*.

- Input impedance* h_{ib} is defined as the ratio of change in the (input) collector voltage with the (input) emitter current I_E kept constant. Therefore,

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E} \quad V_{CB} \text{ constant} \quad (6.14)$$

It is the slope of CB input characteristics I_E versus V_{EB} as shown in Fig. 6.8. The typical value of h_{ib} ranges from 20 Ω to 50 Ω .

- Output admittance* (h_{ob}): It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage with the (input) emitter current I_E kept constant. Therefore,

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}} \quad I_E \text{ constant} \quad (6.15)$$

It is the slope of CB output characteristics I_C versus V_{CB} as shown in Fig. 6.9. The typical value of this parameter is of the order of 0.1 to 10 μ mhos.

- Forward current gain* (h_{fb}): It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) emitter current keeping the (output) collector voltage V_{CB} constant. Hence,

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E} \quad V_{CB} \text{ constant} \quad (6.16)$$

It is the slope of I_C versus I_E curve. Its typical value varies from 0.9 to 1.0.

- Reverse voltage gain* (h_{rb}): It is defined as the ratio of the change in the (input) emitter voltage, and the corresponding change in (output) collector voltage with constant (input) emitter current, I_E . Hence,

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}} \quad I_E \text{ constant} \quad (6.17)$$

It is the slope of V_{EB} versus V_{CB} curve. Its typical value is of the order of 10^{-3} to 10^{-4} .

6.6.2 CE Configuration

Input characteristics To determine the input characteristics, the collector to emitter voltage is kept constant at zero volt and base current is increased from zero in equal steps by increasing V_{BE} in the circuit shown in Fig. 6.10.

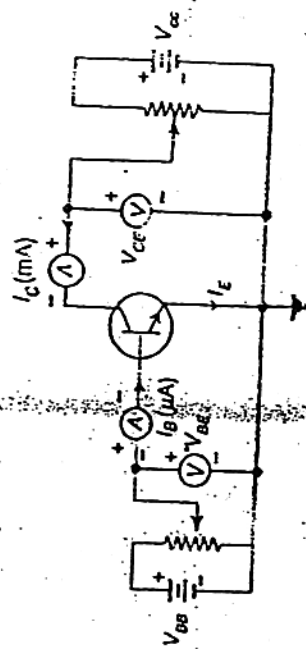


Fig. 6.10 Circuit to determine static characteristics.

The value of V_{BE} is varied for each constant value of V_{CE} .

(iv) Reverse voltage gain (h_{re}): It is defined as the ratio of the change in the (input) base voltage and the corresponding change in (output) collector voltage with constant (input) base current, I_B . Hence,

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}, I_B \text{ constant} \quad (6.21)$$

It is the slope of V_{BE} versus V_{CE} curve. Its typical value is of the order of 10^{-5} to 10^{-4} .

6.6.3 CC Configuration

The circuit diagram for determining the static characteristics of an NPN transistor in the common collector configuration is shown in Fig. 6.13.

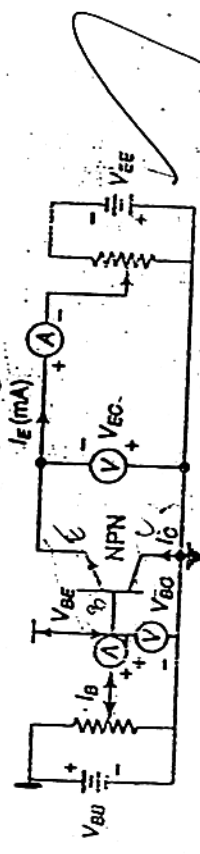


Fig. 6.13 Circuit to determine CC static characteristics

Input characteristics To determine the input characteristics, V_{CE} is kept at a suitable fixed value. The base-collector voltage V_{AC} is increased in equal steps and the corresponding increase in I_B is noted. This is repeated for different fixed values of V_{CE} . Plots of V_{BE} versus I_B for different values of V_{CE} shown in Fig. 6.14 are the input characteristics.

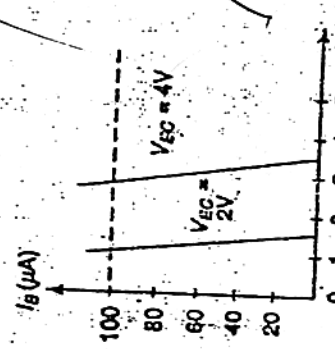
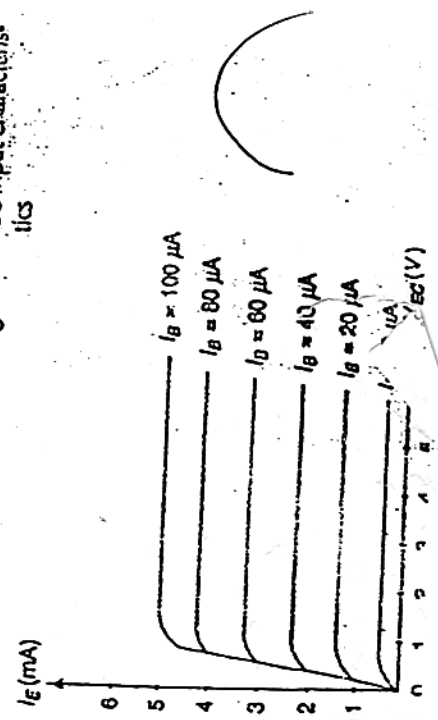


Fig. 6.14 CC input characteristics

Output characteristics The output characteristics shown in Fig. 6.15 are the same as those of the common emitter configuration.



6.6.4 Comparison

Table 6.1 A comparison of CB, CE and CC configurations

Property	CB	CE	CC
Input resistance	Low (about 100 Ω)	Moderate (about 750 Ω)	High (about 750 kΩ)
Output resistance	High (about 450 kΩ)	Moderate (about 45 kΩ)	Low (about 25 Ω)
Current gain	1	High	High
Voltage gain	About 150	About 500	Less than 1
Phase shift between input & output voltages	0 or 360°	180°	0 or 360°
Applications	for high frequency circuits	for audio frequency circuits	for impedance matching

6.6.5 Current Amplification Factor

In a transistor amplifier with a.c. input signal, the ratio of change in output current to the change in input current is known as the current amplification factor.

In the CB configuration the current amplification factor, $\alpha = \frac{\Delta I_C}{\Delta I_E}$ (6.22)

In the CE configuration the current amplification factor, $\beta = \frac{\Delta I_C}{\Delta I_B}$ (6.23)

In the CC configuration the current amplification factor, $\gamma = \frac{\Delta I_E}{\Delta I_B}$ (6.24)

Relationship between α and β We know that $\Delta I_E = \Delta I_C + \Delta I_B$

By definition, $\Delta I_C = \alpha \Delta I_E$

Therefore, $\Delta I_E = \alpha \Delta I_E + \Delta I_B$

i.e. $\Delta I_B = \Delta I_E (1 - \alpha)$

Dividing both sides by ΔI_C , we get

$$\frac{\Delta I_B}{\Delta I_C} = \frac{\Delta I_E}{\Delta I_C} (1 - \alpha)$$

Therefore,

$$\frac{1}{\beta} = \frac{1}{\alpha} (1 - \alpha)$$

$$\beta = \frac{\alpha}{(1 - \alpha)}$$

Rearranging, we also get $\alpha = \frac{\beta}{(1 + \beta)}$ or $\frac{1}{\alpha} = 1 + \beta$ (6.25)

Essentials of a Transistor Biasing circuit

The Biasing circuit associated with the transistor should meet the following requirements.

1. It should ensure proper zero signal collector current.
2. It should ensure that V_{CE} does not fall below 0.5V for Ge transistors & 1V for Si transistors at any instant.
3. It should ensure a fixed (stabilised) operating point.

Stability factor (S)

Defined as the rate of change of collector current I_C with respect to the collector base leakage current I_{CO} having base-emitter voltage V_{BE} and current gain β as constant.

$$S = \left. \frac{\partial I_C}{\partial I_{CO}} \right|_{\beta, V_{BE} = \text{constant}}$$

The collector current for a common emitter amplifier is

$$I_C = \beta I_B + (1 + \beta) I_{CO}$$

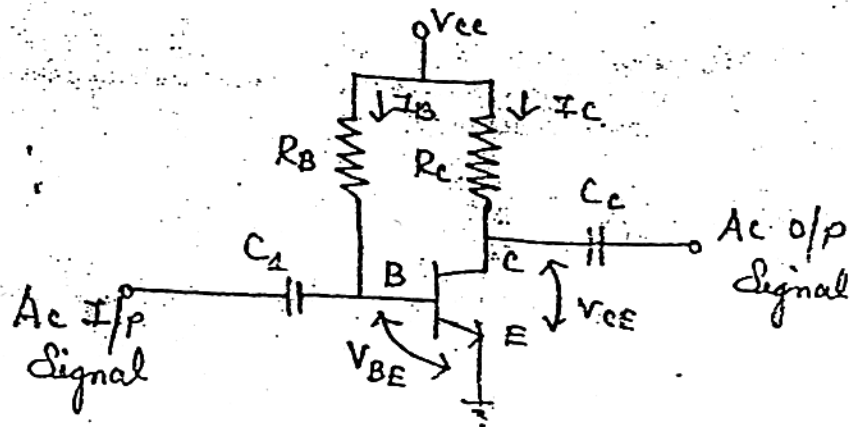
Differentiating the above equation w.r.t I_C ,

$$\frac{I_C}{I_C} = \beta \frac{\partial I_B}{\partial I_C} + (1 + \beta) \frac{\partial I_{CO}}{\partial I_C}$$

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1 + \beta) \frac{\partial I_{CO}}{\partial I_C}$$

- (i) Fixed bias (or) Base resistor Method
- (ii) Fixed bias With emitter resistor
- (iii) Collector to Base bias (or) Biasing With feedback Resistor
- (iv) Collector - emitter feedback bias
- (v) Voltage - divider bias (or) Self bias.

Fixed Bias



Fixed Bias also called as fixed current bias or Base resistor biasing circuit.

Biasing Voltage V_{CC} , V_{BE} & base resistor R_B , Collector resistor R_C are constant quantities. Hence Base current I_B remains fixed at particular level. So it is called fixed Biasing.

Therefore Resistor R_B is selected to obtain the desired level of I_B .

R_B - connected between +ve end of Supply and Base terminal.

To find S'' : $S'' = \frac{\partial I_C}{\partial \beta}$

$$S'' = I_B + \beta \cdot \frac{dI_B}{d\beta} \quad \dots (5)$$

now differentiate equ (2) w.r.t β we get

$$\frac{dI_B}{d\beta} = \frac{d}{d\beta} \left[\frac{V_{CC} - V_{BE}}{R_B} \right] = 0$$

substitute $\frac{dI_B}{d\beta}$ in equ (5) we get

$$S'' = I_B + \beta(0) = I_B \quad (\text{or}) \quad \frac{I_C}{\beta} \left(\frac{s}{1+\beta} \right)$$

Collector to Base Bias:

In collector to base bias circuit the biasing resistor is connected between the collector and the base of the transistor to provide a feedback path.

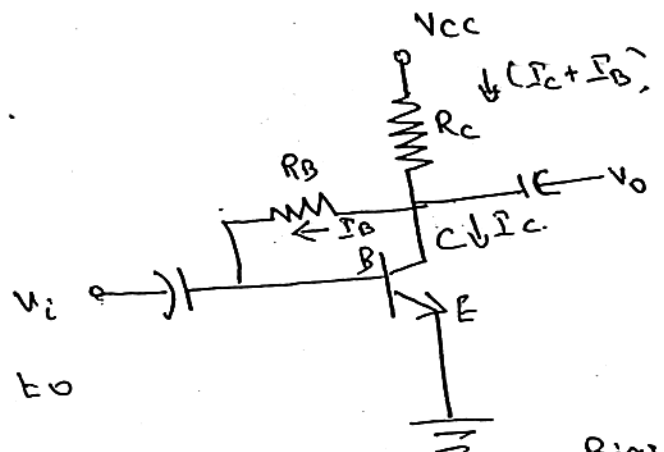
Thus I_B flow through R_B and $(I_C + I_B)$ flow through the R_C .

Stability factors:

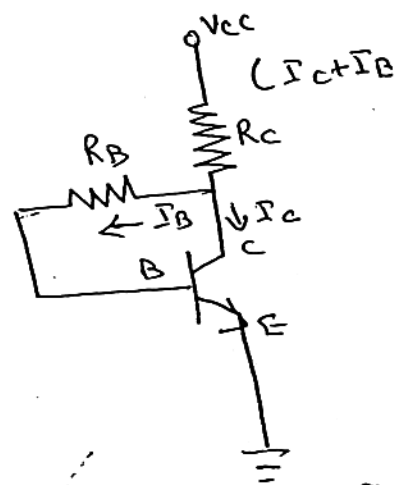
To find S :

Apply KVL to the base of the circuit we get.

$$V_{CC} = [I_C + I_B] R_C + I_B R_B + V_{BE} \quad \dots (1)$$



(Collector - Base Bias)



(DC equivalent circuit)

To find s' :

Consider eqn (4) and differentiate it w.r.t. V_{BE}
we get

$$\frac{dI_B}{dV_{BE}} = \frac{-1}{(1+\beta)R_C + R_B}$$

w.r.t $s' = \beta \cdot \frac{dI_B}{dV_{BE}} = \frac{-\beta}{(1+\beta)R_C + R_B} \quad \text{---(1)}$

To find s'' :

Consider eqn (4) and differentiate it w.r.t. β .

we get.

$$\begin{aligned}\frac{dI_B}{d\beta} &= \frac{d}{d\beta} \left[\frac{V_{CC} - V_{BE}}{(1+\beta)R_C + R_B} \right] \\ &= (V_{CC} - V_{BE}) \frac{d}{d\beta} \left[\left[(1+\beta)R_C + R_B \right]^{-1} \right] \\ &= (V_{CC} - V_{BE}) \cdot -1 \left[(1+\beta)R_C + R_B \right]^{-2} (R_C) \\ &= \frac{-[V_{CC} - V_{BE}] R_C}{[(1+\beta)R_C + R_B]^2}\end{aligned}$$

$$\begin{aligned}\text{w.r.t. } s'' &= I_B + \beta \frac{dI_B}{d\beta} = \frac{V_{CC} - V_{BE}}{(1+\beta)R_C + R_B} - \frac{\beta R_C (V_{CC} - V_{BE})}{[(1+\beta)R_C + R_B]^2} \\ &= \frac{(V_{CC} - V_{BE})(1+\beta)R_C + R_B - \beta R_C [V_{CC} - V_{BE}]}{[(1+\beta)R_C + R_B]^2} \\ &= \frac{(V_{CC} - V_{BE}) [R_C + \cancel{\beta R_C} + R_B - \cancel{\beta R_C}]}{[(1+\beta)R_C + R_B]^2}\end{aligned}$$

Apply KVL to Base to emitter loop we get.

$$V_T = R_B I_B + I_E R_E + V_{BE} \quad \text{--- (1)}$$

$$\text{where as } I_E = I_B + I_C$$

$$V_T = (R_B + R_E) I_B + I_C R_E + V_{BE}$$

$$\therefore V_T - V_{BE} - I_C R_E = (R_B + R_E) I_B \quad \text{--- (2)}$$

$$I_B = \frac{(V_T - V_{BE})}{(R_B + R_E)} - \frac{I_C R_C}{(R_B + R_E)} \quad \text{--- (3)}$$

$$\text{(or) substitute } I_C = \beta I_B \text{ in}$$

equ (2) we get.

$$V_T - V_{BE} = [(1 + \beta) R_E + R_B] I_B$$

$$I_B = \frac{V_T - V_{BE}}{[(1 + \beta) R_E + R_B]} \quad \text{--- (4)}$$

we consider equ (3) for our analysis.

Consider equ (3) and diff it w.r.t to

I_C we get.

$$\frac{dI_B}{dI_C} = - \frac{R_C}{R_B + R_E}$$

$$\text{w.k.t } S = \frac{1 + \beta}{1 - \beta \left(\frac{dI_B}{dI_C} \right)} = \frac{1 + \beta}{1 + \beta \left(\frac{R_C}{R_B + R_E} \right)} //$$

Consider equ (80)

$$V_T = \frac{(R_B + R_E) I_C}{\beta} - \frac{(1+\beta) I_{CO} (R_B + R_E)}{\beta} + V_{BE} + I_C R_E$$
$$= \frac{[R_B + (1+\beta) R_E] I_C}{\beta} - \frac{(1+\beta) I_{CO} [R_B + R_E]}{\beta} + V_{BE}$$

$$V_T - V_{BE} + \frac{(1+\beta) I_{CO} [R_B + R_E]}{\beta} = \frac{[R_B + (1+\beta) R_E] I_C}{\beta}$$

$$\therefore I_C = \frac{(V_T - V_{BE}) \beta}{[R_B + (1+\beta) R_E]} + \frac{\cancel{\beta} (1+\beta) I_{CO} (R_B + R_E)}{\cancel{\beta} [R_B + (1+\beta) R_E]}$$

$\beta \gg 1$ so in only numerator replace $(1+\beta) =$

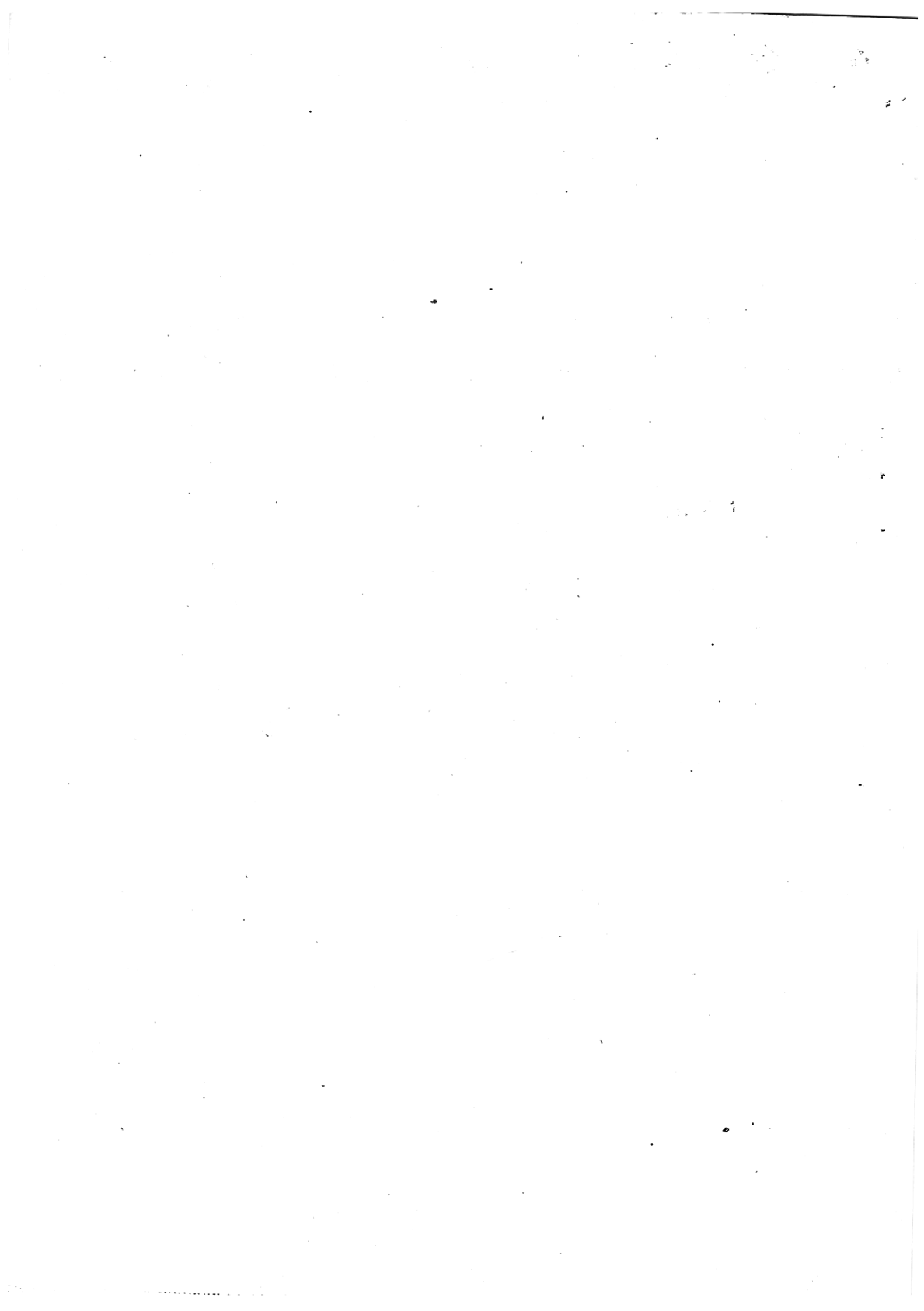
$$\therefore I_C = \frac{(V_T - V_{BE}) \beta}{R_B + (1+\beta) R_E} + \frac{\beta I_{CO} (R_B + R_E)}{[R_B + (1+\beta) R_E]}$$

$$I_C = \frac{\beta [V_T - V_{BE} + I_{CO} (R_B + R_E)]}{R_B + (1+\beta) R_E}$$

differentiate I_C w.r.t. β we get.

$$\frac{dI_C}{d\beta} = [V_T - V_{BE} + I_{CO} (R_B + R_E)] \cdot \frac{d}{d\beta} \left[\frac{\beta}{R_B + (1+\beta) R_E} \right]$$

it is in the form $\frac{U}{V}$ method.



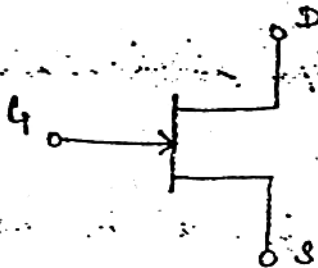
Source (S) / Drain (D) - The terminals through which the major carrier enters the bar.

Denoted as I_s / $-I_D$.

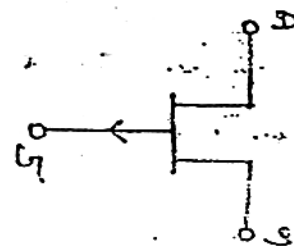
Gate (G) - Heavily doped region, designated as I_G .

Channel - The region in the semiconductor bar between the two gate regions through which major carriers move from source to drain.

JFET
Symbol



n-channel JFET



p-channel JFET

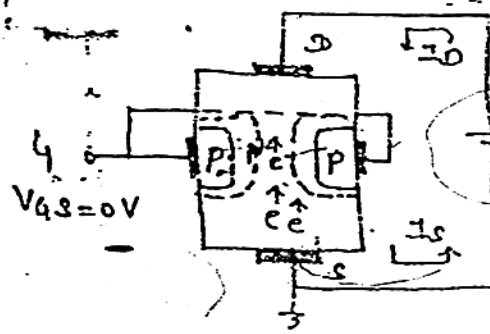
* Drain and Source terminals can be ~~used~~ interchanged.

(i) $V_{GS} \geq 0$, $V_{DS} \geq 0$

[Not for analog modes]

operation of JFET

(ii) $V_{GS} = 0$, $V_{DS} \neq 0$ (Some positive value)



pinch off condition
 $V_{DS} = V_p$

When a reverse Voltage V_{GS} is applied between gate & Source, the Width of the depletion layer increases

This reduces the Width of the conducting channel. So current from source to drain is decreased

If reverse Voltage V_{GS} is decreased, the Width of Conducting Channel is increased and so current from source to drain is increased.

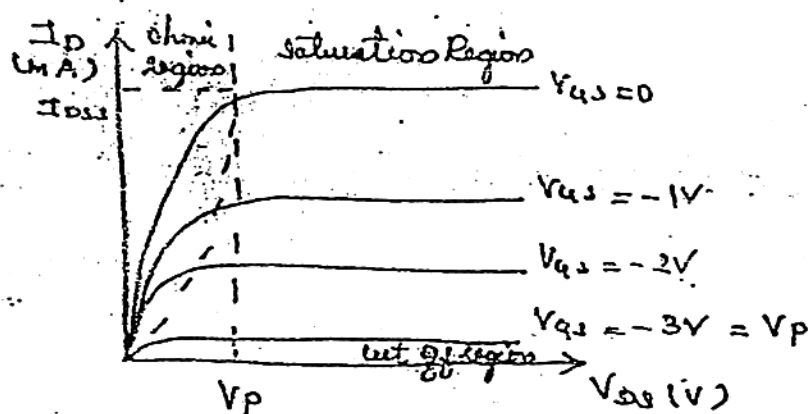
From this we infer that current is controlled by gate potential hence Voltage Controlled device.

When V_{GS} applied d.r ↑, s → d ↓.

JFET Characteristics

$V_{GS} ↓$, width of channel ↑, s → d ↑.

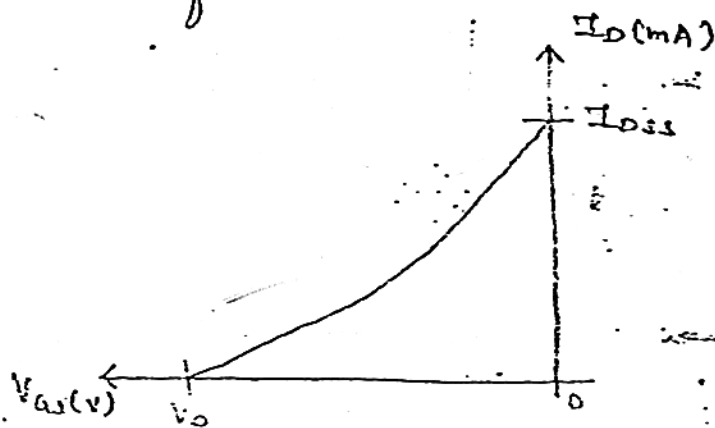
Drain Characteristics



* I_D versus V_{DS} for different values of V_{GS}

* I_D becomes constant. V_{GS} is increased

Transfer Characteristics



Transfer characteristics is given by Shockley

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_0}\right)^2$$

for $V_{GS} = 0V$, $I_D = I_{DSS}$

for $V_{GS} = V_P$, $I_D = 0$

Ratio of Small change in drain current to the Small change in gate to source Voltage at Constant drain Voltage. Unit of Conductance / transconductance is mho -

Drain resistance (r_d)

$$r_d = \left(\frac{\partial V_{DS}}{\partial I_D} \right)_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \Big|_{V_{GS} = \text{constant}}$$

Ratio of Small change in drain to source Volt to change in drain current at Constant gate to source Voltage. Unit of resistance is ohms (Ω).

Amplification factor (μ)

$$\mu = \left(\frac{\partial V_{DS}}{\partial V_{GS}} \right)_{I_D} = \frac{\Delta V_{DS}}{\Delta V_{GS}} \Big|_{I_D = \text{constant}}$$

Ratio of Small change in drain Voltage to Small change in gate to source Voltage at Constant drain

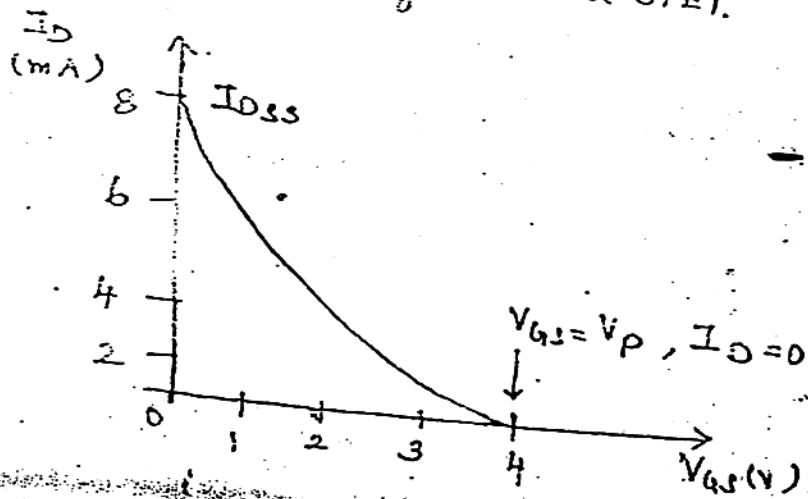
Relationship among parameters

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\boxed{\mu = r_d \times g_m}$$

TRANSFER characteristics of P-channel JFET.



$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

I_D & I_{DSS} are reversed in directions, V_{GS} & V_P are positive for P channel JFET.

Applications of FET

- * Used as buffer in measuring Instruments
- * In RF Amplifiers, cascade, low frequency Amplifiers
- * FM tuners
- * Mixer & Oscillator circuits
- * Digital circuits
- * As Variable resistor.

Advantages of JFET

- * High Input resistance
- * Small size
- * Longevity (long life)
- * Low Noise
- * Better Thermal Stability
- * High frequency response & High immunity to radiation

Applying KVL

$$-V_{Gg} - V_{Gs} = 0$$

$$\therefore, V_{Gs} = -V_{Gg}$$

V_{Gg} is fixed in dc supply, V_{Gs} is fixed in magnitude resulting in the designation Fixed-Bias Configuration.

The resulting level of drain current I_D is controlled by Shockley's equation

$$I_D = I_{DSS} \left(1 - \frac{V_{Gg}}{V_P} \right)^2$$

$$V_{Gs} = -V_{Gg}$$

$$I_D = I_{DSS} \left(1 + \frac{V_{Gs}}{V_P} \right)^2$$

* Drain-to-Source Voltage of output section

Apply KVL

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$(or) V_{DS} = V_{DD} - I_D R_D$$

$$W.K.T \quad V_S = 0 \quad (\text{single subscript})$$

$$V_{DS} = V_D - V_S \quad (\text{double subscript})$$

$$V_D = V_{DS} + V_S = V_{DS} + 0V$$

$$\boxed{V_D = V_{DS}}$$

$$V_{Gs} = V_G - V_S$$

$$V_G = V_{Gs} + V_S = V_{Gs} + 0V$$

$$\boxed{V_G = V_{Gs}}$$

0 - source loop

$$-V_{GS} - V_{RS} = 0$$

and $V_{GS} = -V_{RS}$

or $V_{GS} = -I_D R_S$

Drain current I_D

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

$$I_D = I_{DSS} \left(1 - \frac{-I_D R_S}{V_P} \right)^2$$

$$I_D = I_{DSS} \left(1 + \frac{I_D R_S}{V_P} \right)^2$$

Drain Source Voltage V_{DS}

$$V_{DD} - V_{RD} - V_{DS} - V_{RS} = 0$$

$$V_{DS} = V_{DD} - V_{RS} - V_{RD}$$

$$V_{DS} = V_{DD} - I_S R_S - I_D R_D$$

but $I_D = I_S$

$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$

but $V_S = I_D R_S$

$$V_G = 0V$$

$$V_D = V_{DS} + V_S = V_{DD} - I_D R_D$$

$$V_{DS} = V_{DD} - I_D [R_D + R_S]$$

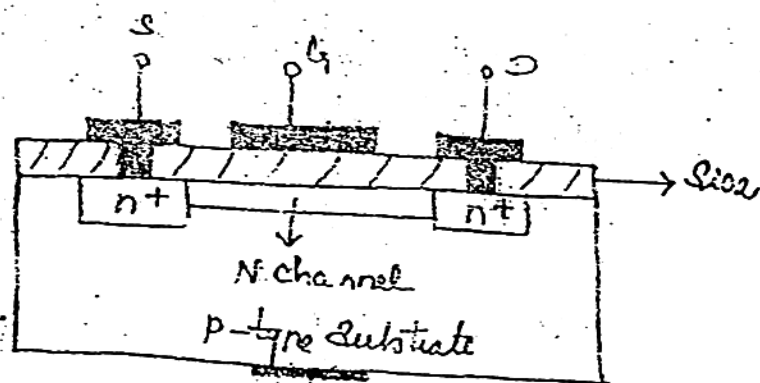
Q points are -

$$I_{DQ} = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

• Where $V_{GS} = V_G - I_D R_S$

~~$$V_{DSQ} = V_{DD} - I_D (R_D + R_S)$$~~

Construction



B/Ss

B - Bulk

Ss - Substrate

P-type Material forms Substrate. Two highly doped n+ regions diffused into a lightly doped Substrate.

One n+ region is called Source (S) and other n+ region is called Drain (D).

In between two n+ regions is Channel. And the metal that covers the Channel is gate (G).

Operation

The depletion MOSFET can be operated in two different modes.

- (i) Depletion mode
- (ii) Enhancement mode.

Depletion mode

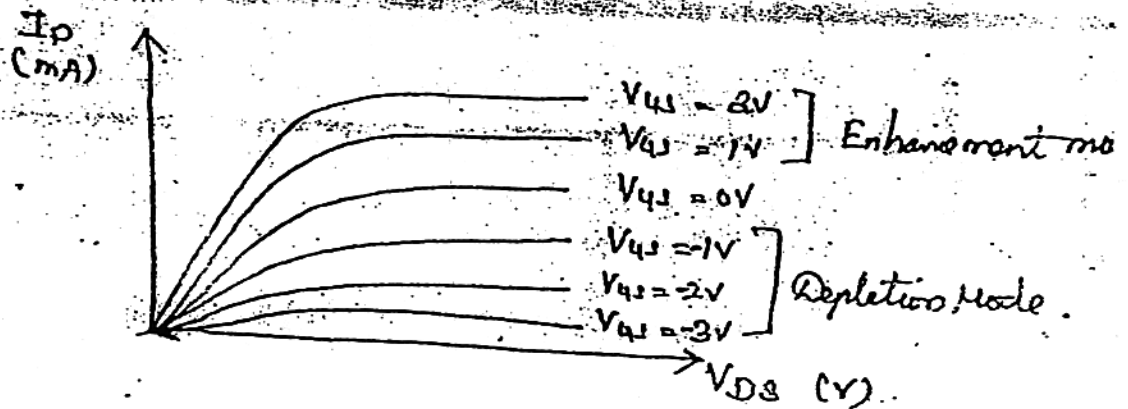
Gate terminal is negative w.r.t Source and D is positive w.r.t Source.

$$V_{GS} = -ve$$

$$V_{DS} = +ve$$

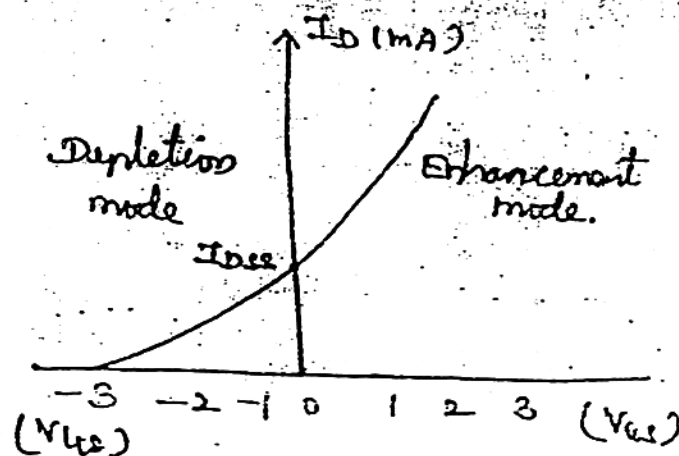
Then depletion MOSFET can be operated in both depletion mode & enhancement mode by applying negative & positive Voltage on g . Also, the depletion MOSFET conducts even if the gate to Source Voltage is Zero. Hence called as Normally ON MOSFET.

Drain Characteristics



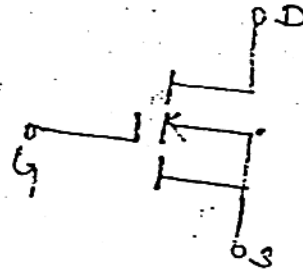
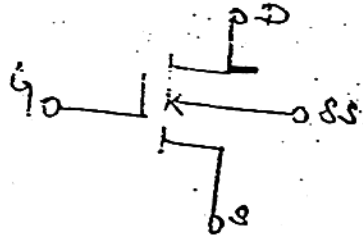
Drain characteristics is graph between I_D (V_{DS}) V_{GS} at Constant V_{GS} .

Transfer Characteristics

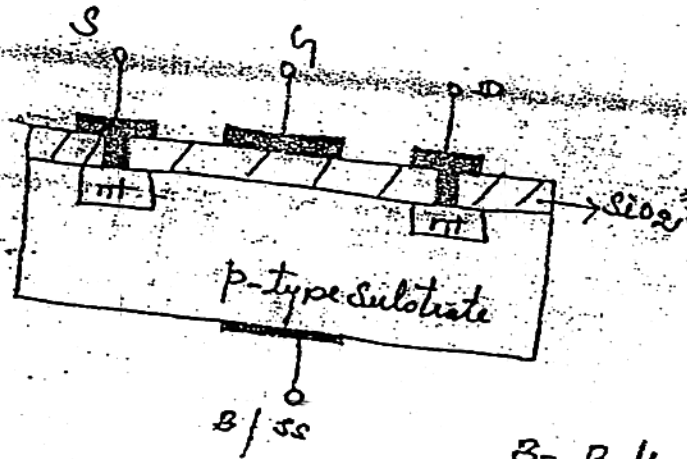


The curve of I_D versus V_{GS} for constant V_{DS} is called the transfer characteristics of MOSFET.

n Channel Enhancement MOSFET



Construction



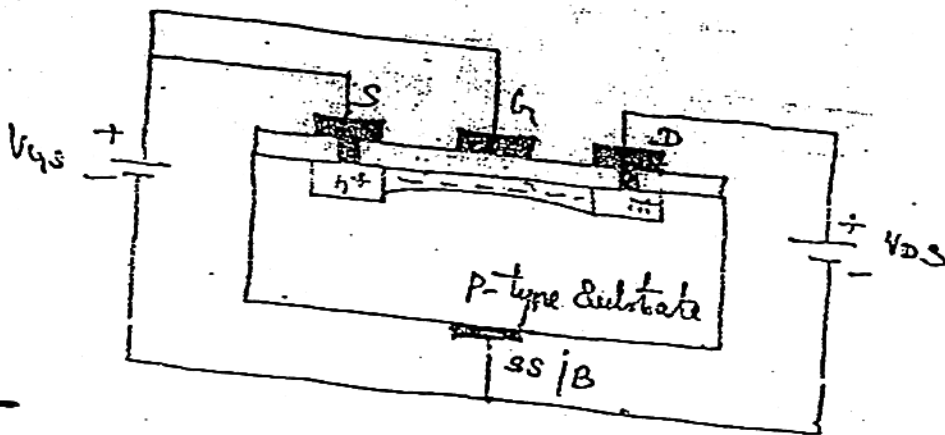
B - Bulk
SS - Substrate

pure material forms substrate, Two highly doped n⁺ regions are diffused into a lightly doped substrate.

One n⁺ region is called Source (S) and other n⁺ region is called Drain (D).

Third terminal is Gate (G).

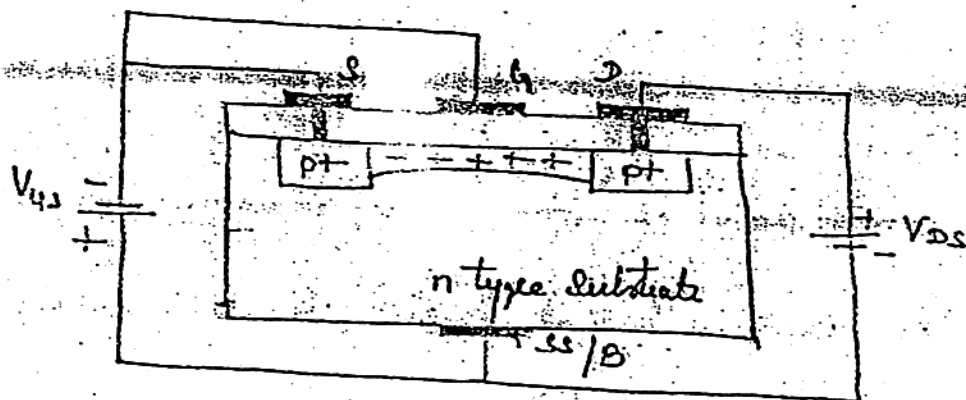
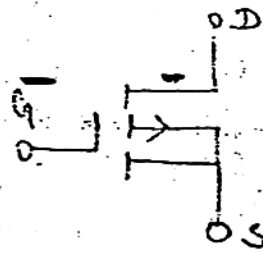
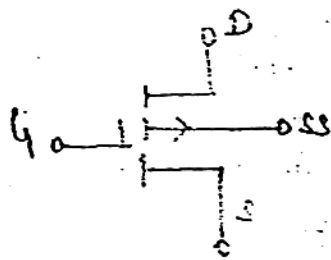
Operation



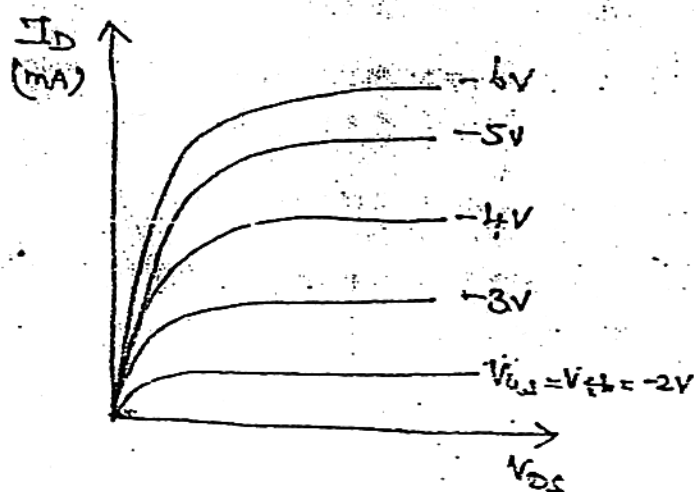
* Inversion (V_{GS} is large positive) :-
~~~~~

The conducting path occurs between the source and drain. This conducting path is called channel and the condition is called inversion.

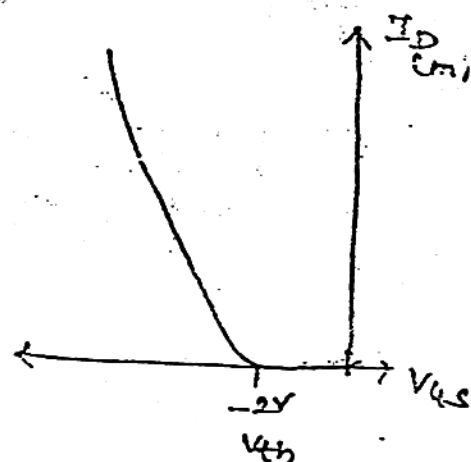
\* P Channel enhancement type MOSFET



## • Plain Characteristics



## Transfer Characteristics

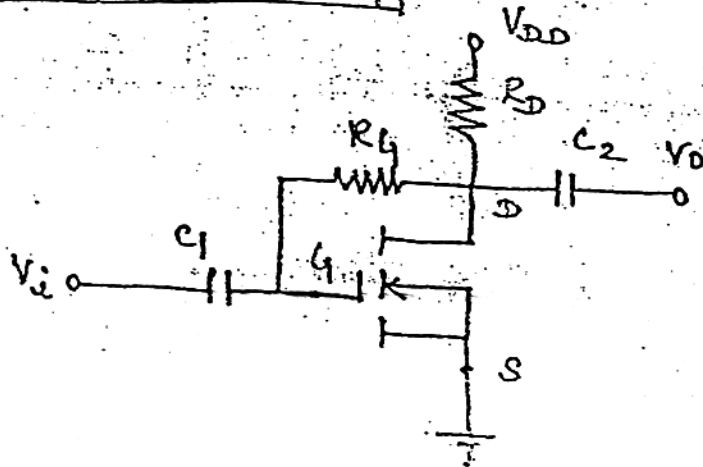


$$k = \frac{I_{D(on)}}{[V_{GS(on)} - V_{GS(th)}]^2}$$

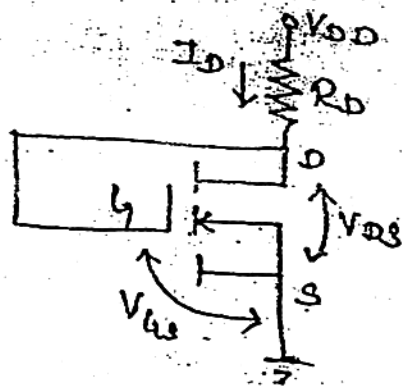
The power dissipated in the transistor, Since there is no gate current is

$$P_T = I_D V_{DS}$$

1. Feedback biasing



DC equivalent Network / DC Analysis



$$I_G = 0, V_{R_G} = 0$$

$$\therefore V_D = V_G$$

$$\text{and } V_{DS} = V_{GS}$$

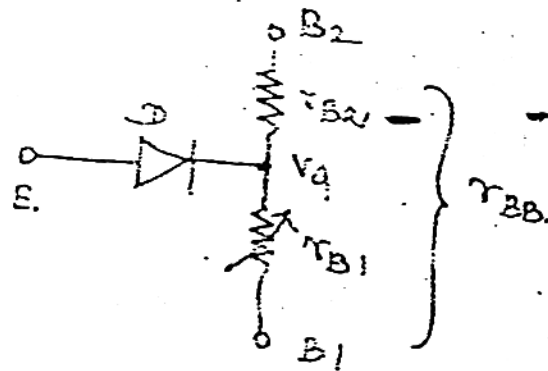
For output circuit

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{GS} = V_{DD} - I_D R_S$$



6/11/97



- \* Consists of diode + Resistance
- \* Diode represents PN Junction, Resistance  $r_{B1}$  &  $r_{B2}$  is the internal bulk resistance.
- \*  $r_{BB}$  - Total resistance / Interbase resistance.

$$r_{BB} = r_{B1} + r_{B2}$$

$r_{B1}$  - bulk resistance between emitter (E) and base 1 ( $B_1$ ),

$r_{B2}$  - bulk resistance between emitter (E) and base 2 ( $B_2$ ).

\* When no voltage applied,  $r_{BB}$  is 5 to 10k $\Omega$ .

\*  $r_{B1}$  is variable resistance, because  $r_{B1}$  is inversely proportional to emitter current  $I_E$ .

So depending upon the values of emitter current  $r_{B1}$  varies from  $4k\Omega$  to  $40\Omega$ .

### Intensity stand off ratio

The resistance ratio  $\frac{r_{B1}}{r_{BB}}$  is known as intensity stand-off ratio. ( $\eta$ ).

$$\eta = \frac{r_{B1}}{r_{BB}} = \frac{r_{B1}}{r_{B1} + r_{B2}} \quad \frac{V_P - V_V}{V_{BB}}$$

→ small emitter current flows from  $B_2$  to  $B_1$ , due to minority carriers.

As long as the applied emitter voltage is below the total reverse bias voltage i.e.  $(2V_{BB} + V_D)$ , the diode is reverse bias.

Once applied emitter voltage is greater than  $2V_{BB} + V_D$  the diode conducts & emitter current flows.

The value of emitter voltage which causes the diode to conduct is called peak-point voltage ( $V_p$ ).

\* Diode conducts - forward biased - UJT is triggered ON.

(i) holes are injected into N-type Bar. (holes repelled by  $B_2$  terminal and attracted by  $B_1$  terminal)

(ii) Excess holes, reduces  $\tau_{B1}$ .

(iii) Reduction in  $\tau_{B1}$ , reduces intrinsic stand-off voltage ( $\eta \cdot V_{BB}$ ).

(iv)  $\therefore$  emitter current increases, while emitter voltage ( $V_E = 2 \cdot V_{BB} + V_D$ ) decreases.

This produces Negative resistance Region.

(UJT switches from OFF to ON state)

... case in which current is due to ... in ...  
resistance  $r_B$ ). Some call it as Negative resistance region.

Saturation region.

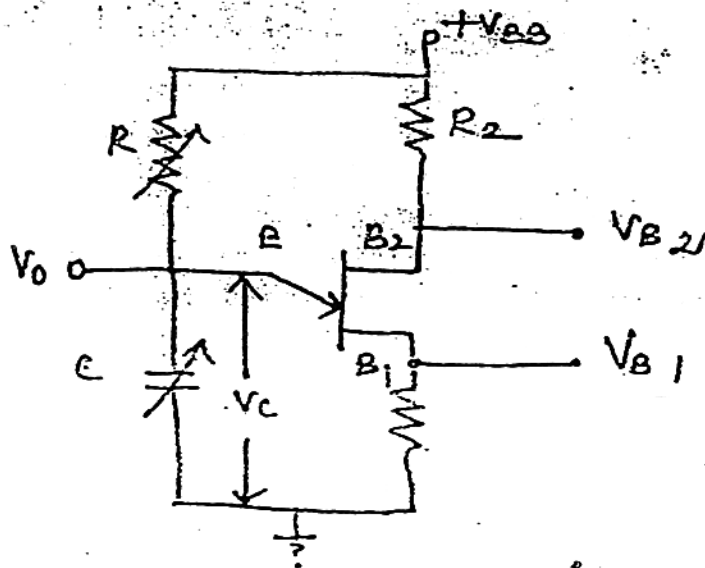
region & the Valley point is called Saturation region. Device is ON this region.

Emitter stage  $V_E$  remains almost constant with the increasing emitter current.

Applications of UJT:-

- \* Trigger device for SCRs + TRIACs
- \* Non-Sinusoidal Oscillators.
- \* Saw tooth generators
- \* Timing circuits.

UJT as Relaxation oscillator



7-8 --- unions

Initially capacitor is uncharged. Voltage across capacitor before breakdown.

$$V_c = V_v + V_{BB} (1 - e^{-t/Rc}) \rightarrow 1.$$

Discharge of capacitor

$$V_p = V_o + \eta \cdot V_{BB} \rightarrow 2.$$

ie.,  $V_p = V_c$

$$\therefore V_v + V_{BB} (1 - e^{-t/Rc}) = V_o + \eta \cdot V_{BB}$$

Neglecting  $V_o + V_v$

$$\eta V_{BB} = V_{BB} (1 - e^{-t/Rc})$$

$$e^{-t/Rc} = 1 - \eta$$

Take log on both sides

$$\ln(e^{-t/Rc}) = \ln(1 - \eta)$$

$$\frac{-t}{Rc} = \ln(1 - \eta)$$

$$t = -Rc \ln(1 - \eta)$$

$$t = Rc \ln(1 - \eta)^{-1}$$

$$t = Rc \ln \frac{1}{1 - \eta}$$

$$t = 2.303 Rc \log_{10} \frac{1}{1 - \eta}$$

If discharge time is neglected,  $t - T$ , period of wave  $\therefore$  The frequency of oscillations of sawtooth wave.

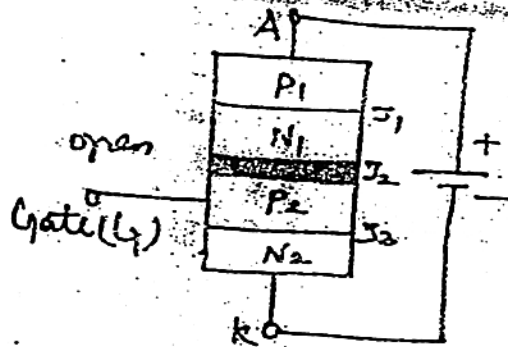
$$f = \frac{1}{T} = \frac{1}{2.303 Rc \log_{10} \left( \frac{1}{1 - \eta} \right)}$$

- (i) four semiconductor layers PNPN
- (ii) Three junctions  $J_1, J_2, J_3$
- (iii) Three terminals Anode, Cathode & Gate

Working / operation

(i) Gate is open,

Anode is positive with respect to Cathode.



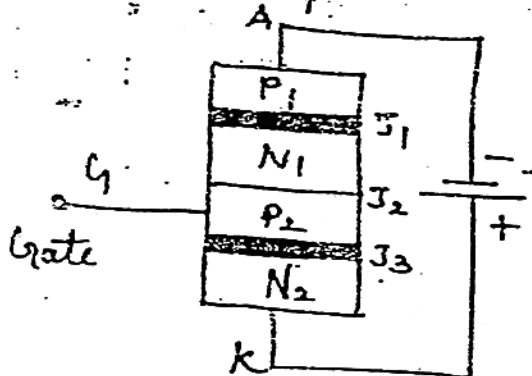
$J_1$  &  $J_3$  — forward biased  
 $J_2$  — reverse biased

∴ Set-off state, only leakage current flows. This region is called forward blocking region.

Voltage applied to anode and cathode is called forward voltage.

(ii) Gate "open"

Cathode positive with respect to Anode



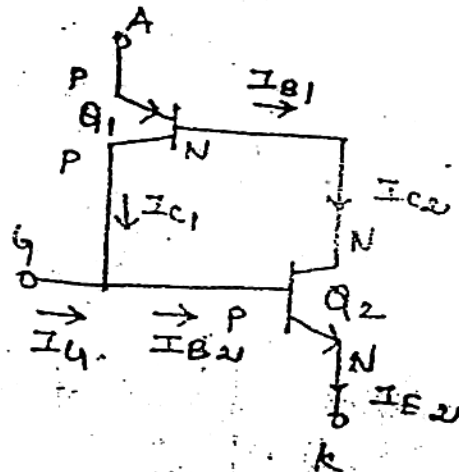
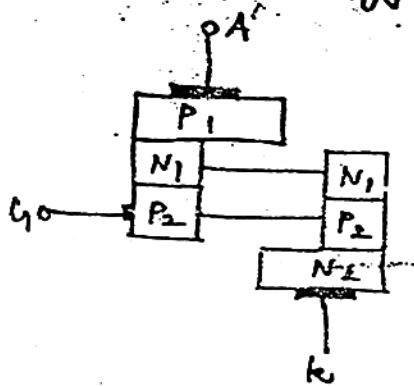
$J_1$  &  $J_3$  Reverse biased  
 $J_2$  — forward biased

increases, more electrons cross junction.  
 $I_2$ , anode current further increases  $\rightarrow$   $J_2$  junction breaks  
 and SCR conducts heavily.

If anode to cathode voltage is reversed, the device enters into reverse blocking region.

Increase in reverse voltage leads to Breakdowns called reverse breakdown voltage.

Two transistor analogy (SCR equivalent circuit)



Collector terminal of each transistor is connected to base terminals.

$$\text{ie } I_{C1} = I_{B2}$$

$$I_{C2} = I_{B1}$$

Current going to  $I_G$  is the base current of  $Q_2$ .

If base current increases, collector current increases for  $Q_2$ .  
 Therefore base current increases for  $Q_1$ , and leads to increase in collector current of  $Q_1$ .

SCR - ON state. (Current passes from Anode to Cathode)

As the reverse voltage  $V_R$  is increased from zero, a very little current flows.

SCR  $\rightarrow$  OFF State

If reverse voltage is greater than  $V_{BR}$ , current increases rapidly. (breakdown of SCR occurs - damage device)

OD region — reverse blocking region.

DE region — reverse avalanche region.

Triggering ON (or) Turning ON SCR.

1. Forward breakover Voltage

Voltage across the SCR exceeds the forward breakover voltage, the SCR will start conduction.

2. Gate triggering

used to trigger SCR ON. Once the gate has no further control on the device current.  $\uparrow$  SCR is ON

3. Rate effect or  $\frac{dv}{dt}$  triggering

By increasing the anode to cathode voltage, SCR turns ON.

voltage increases, produces a charging current, which triggers SCR to conduction.

4. Light triggering

SCR turned ON by light falling on J<sub>2</sub> Junction of SCR. (Light activated SCR).

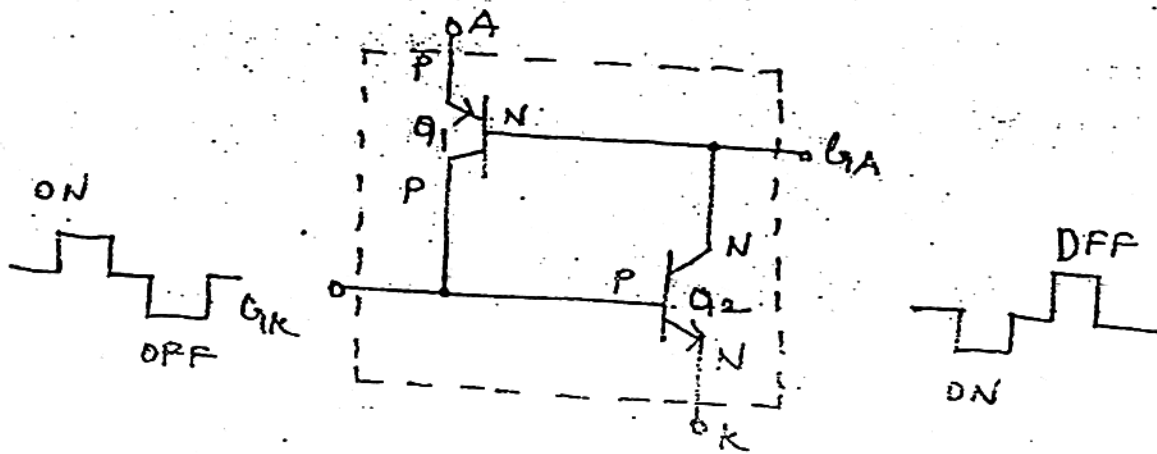


Anode A  
 Cathode K  
 Anode Gate  $G_A$   
 Cathode Gate  $G_K$

Advs:-

SCS can be turned ON & OFF using either gate terminal. But in SCR can be turned ON only using its gate terminal.

operation



Initially  $Q_1$  &  $Q_2$  are OFF. SCS is OFF.

If a positive pulse is applied on cathode gate  $G_K$ ,  $Q_2$  will be driven into conduction,  $\therefore$  it provides a base current to transistor  $Q_1$ .

$Q_1$  turns ON.

Collector current of  $Q_2$  drives  $Q_1$  transistor.

$\therefore$  Both  $Q_1$  &  $Q_2$  moves to Saturation. Hence SCS turns ON by applying negative pulse (ON) at the anode gate terminal.

For turning OFF. Apply positive pulse (OFF) at anode gate terminal and negative pulse (OFF) at Cathode gate terminal.

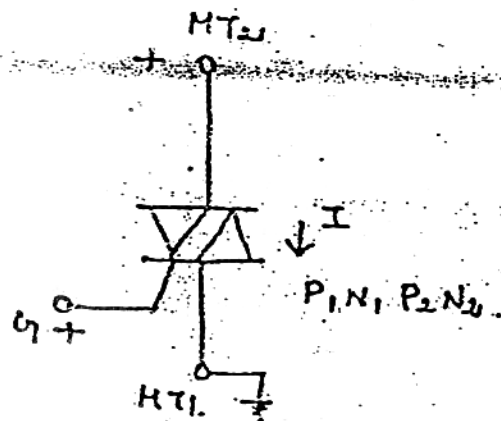
Currents & voltages as per axes

\*  $P_1, N_1, P_2, N_2$

\*  $P_2, N_1, P_1, N_2$

3 terminals are  $MT_1$ ,  $MT_2$ , and Gate terminal

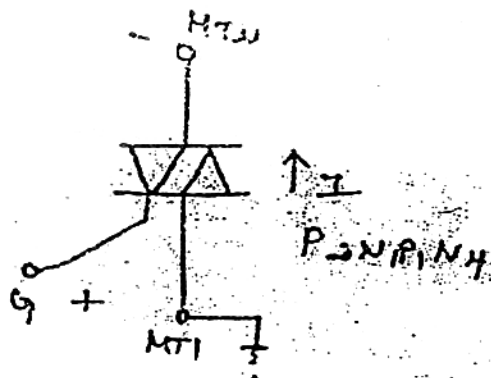
operation



1.  $MT_2$  is positive &  $G$  is positive

Current flows from  $MT_2$  to  $MT_1$  i.e.,  
 $P_1, N_1, P_2, N_2$ .

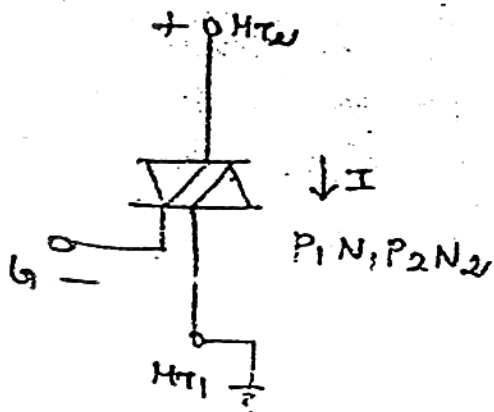
In this mode Triac operation is identical to SCR.



2.  $MT_2$  is Negative &  $G$  is positive

Current flows from  $MT_1$  to  $MT_2$  i.e.,  
 $P_2, N1, P1, N2$ .

inefficient mode & must be avoided

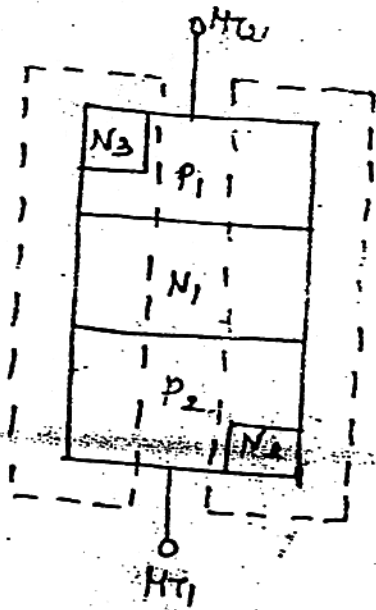


3.  $MT_2$  is Positive &  $G$  is Negative

Current flows from  $MT_2$  to  $MT_1$  i.e.,  
 $P_1, N1, P_2, N_2$ .

less efficient than mode 1

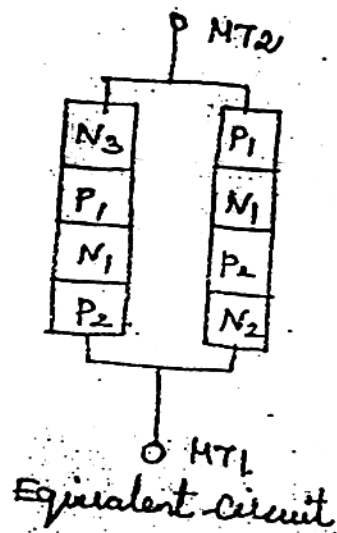
Two terminal, three layer, bidirectional device (DIAC).



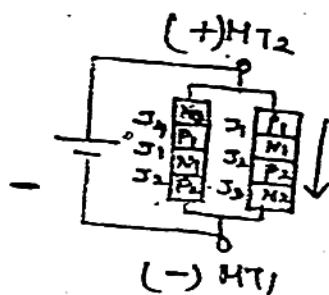
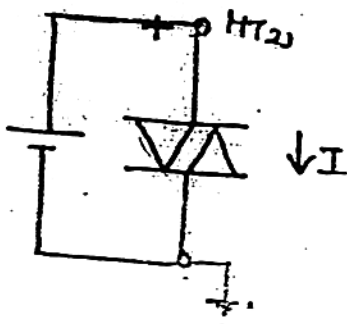
\* Consists of two 4 layer diodes connected in parallel but in opposite directions

$P_1 N_1 P_2 N_2$

$P_2 N_1 P_1 N_3$



operation



When the applied voltage is positive  $HT_2$  with respect to  $HT_1$ , diode conducts and current passes through the diode  $P_1 N_1 P_2 N_2$  from  $HT_2$  to  $HT_1$

$J_2, J_4$  - reverse biased

$J_1, J_3$  - forward biased.

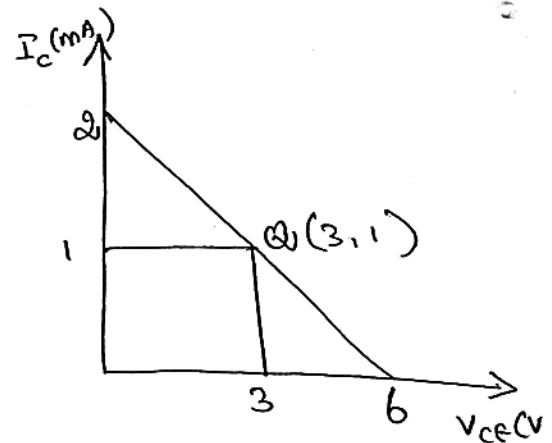


$$V_{CE} = V_{CC} - I_C R_C$$

when  $I_C = 0$  then  $V_{CE} = V_{CC} = 6V$

Similarly  $V_{CE} = 0$  then  $I_C = \frac{V_{CC}}{R_C}$

$$I_C = \frac{V_{CC}}{R_C} = \frac{6}{3 \times 10^3} = 2 \text{ mA}$$



(b) Operating point Q:

For Silicon transistor  $V_{BE} = 0.7V$

$$V_{CC} = I_B R_B + V_{BE}$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{6 - 0.7}{530 \times 10^3} = 10 \mu A$$

$$\therefore I_C = \beta I_B = 100 \times 10 \times 10^{-6} = 1 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 6 - [1 \times 10^{-3} \times 3 \times 10^3] \\ = 6 - 3$$

$$V_{CE} = 3V$$

$\therefore$  The operating point is  $V_{CEQ} = 3V$  &  $I_{CQ} = 1 \text{ mA}$

(c) Stability factor.  $S = 1 + \beta = 1 + 100 = 101$

Problem 5: Consider a voltage divider bias circuit using BJT where  $V_{CC} = 20V$ ,  $R_C = 2k\Omega$ ,  $\beta = 50$ ,  $V_{BE} = 0.2V$ ,  $R_1 = 100k\Omega$ ,  $R_2 = 10k\Omega$ ,  $R_E = 100\Omega$ . Calculate  $I_B$ ,  $V_{CE}$ ,  $I_C$  and stability factor  $S$ .

Sol:

$$V_T = V_{CC} \cdot \frac{R_2}{R_1 + R_2} = 20 \cdot \frac{10}{100 + 10} = 1.818 \text{ V}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{100 \times 10}{110} = 9.09 \text{ k}\Omega$$

$$I_D = 12 \text{ mA} \left[ 0.0576 I_D^2 \text{ M}\Omega - 0.48 \text{ k} I_D + 1 \right]$$

$$= 0.691 \text{ k}\Omega I_D^2 - 25 I_D + 1$$

$$0 = 0.691 \text{ k}\Omega I_D^2 - 26 I_D + 1$$

$$\left[ \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \right]$$

$$\therefore I_D = 2.33 \text{ mA (or)} 7.45 \text{ mA}$$

Consider  $I_D = 7.45 \text{ mA}$

$$\therefore V_{DS} = V_{DD} - [-I_D (R_S + R_D)]$$

$$= -18 - [-7.45 (1.2 \times 10^3 + 3.3 \times 10^3)]$$

$$= 15.52 \text{ V}$$

But practically  $V_{DS}$  for p-FET should be negative.

$\therefore I_D = 7.45 \text{ mA}$  is invalid.

Now Consider  $I_D = 2.33 \text{ mA}$

$$\therefore V_{DS} = V_{DD} - [-I_D (R_S + R_D)]$$

$$= -18 - [-2.33 \times 10^{-3} (1.2 \times 10^3 + 3.3 \times 10^3)]$$

$$V_{DS} = -18 + 10.485 = -7.515 \text{ V}$$

$$\therefore V_{GS} = I_D R_S = 2.33 \times 10^{-3} \times [1.2 \times 10^3]$$

$$V_{GS} = 2.796 \text{ V}$$

Problem 7: For N-EMOSFET  $V_T = 0.7 \text{ V}$ ,  $W = 30 \mu\text{m}$ ,  $L = 5 \mu\text{m}$   
 $\mu_n = 650 \text{ cm}^2/\text{V}\cdot\text{s}$ ,  $\epsilon_{ox} = 4.50 \times 10^{-8}$ ,  $\epsilon_{ox} = 3.9 \times 8.85 \times 10^{-14} \text{ F/cm}$

Assume transistor is biased in saturation region.

(i) Determine drain current when  $V_{GS} = 2V_T$ .

Assuming transistor is biased in the saturation, the drain current is

$$I_D = K [V_{GS} - V_T]^2 = [0.1 \times 10^{-3}] (4-1)^2 = 0.9 \text{ mA}$$

$$V_{DS} = V_{DD} - I_D R_D = 10 - [0.9 \times 10^{-3} \times 1.5 \times 10^3] = 8.65 \text{ V.}$$

where.  $V_{DS}(\text{sat}) = V_{GS} - V_T = 4 - 1 = 3 \text{ V.}$

ie  $V_{DS} > V_{DS}(\text{sat})$  therefore the transistor is biased in the saturation region.

Problem 10: Determine  $I_{DQ}$ ,  $V_{GSQ}$ ,  $V_D$  and  $V_S$  for the MOSFET circuit shown in Fig. Given for MOSFET  $V_{GS} = 3 \text{ V}$ ,  $I_{D(\text{ON})} = 8 \text{ mA}$  and  $V_{GS(\text{ON})} = 6 \text{ V}$ .

Sol:

$$K = \frac{I_{D(\text{ON})}}{[V_{GS(\text{ON})} - V_T]^2}$$

$$= \frac{5 \times 10^{-3}}{[6 - 3]^2} = 0.55 \text{ mA/V}^2$$

$$V_{G1} = V_G = \left( \frac{R_2}{R_1 + R_2} \right) V_{DD}$$

$$= \left\{ \frac{6.8 \times 10^6}{[10 \times 10^6 + 6.8 \times 10^6]} \right\} 24$$

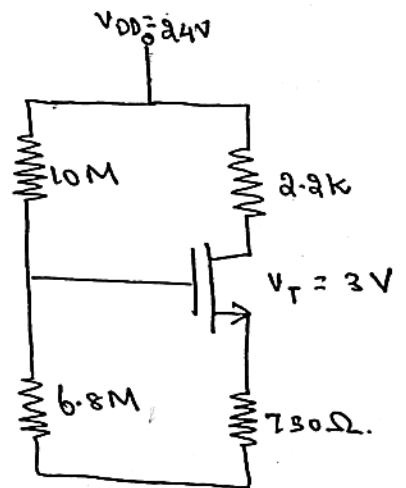
$$V_{G1} = 9.714 \text{ V}$$

To find  $V_{GS}$  Apply KVL to I/p loop we get.

$$V_{G1} = V_{GS} + I_D R_S$$

$$V_{GS} = V_{G1} - I_D R_S = [9.714] - (750) I_D$$

To find  $I_D$ :



### Modes of operation

34 gm

In order to operate transistor as an amplifier the two PN junctions should be properly biased with Voltages. Depending on bias voltage, the transistor operates in one of three regions

1. Active Region
2. Saturation Region
3. Cut off Region

| Mode                 | Emitter - base junction<br>$J_E$ | Collector - base junction<br>$J_C$ |
|----------------------|----------------------------------|------------------------------------|
| 1. Active Region     | Forward bias                     | Reverse bias                       |
| 2. Saturation Region | Forward bias                     | Forward bias                       |
| 3. Cut off Region    | Reverse bias                     | Reverse bias                       |

### Transistor operation

Emitter - base junction of a transistor is forward biased whereas collector - base junction is reverse biased i.e., (Active region). The emitter current almost entirely flows in the collector circuit.

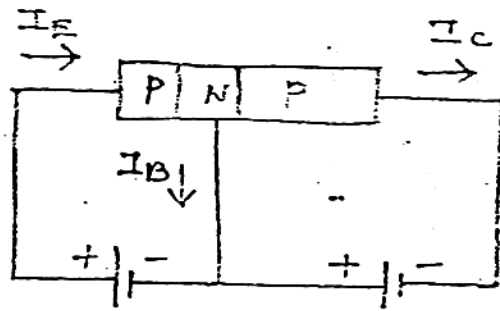
$\therefore$  Collector Current depends on emitter current.  
This is the operation of Transistor. (Internal function).



## Working of pnp transistor

35

SM



\* Emitter-base junction is forward biased

\* Collector-base junction is reverse biased

The forward bias causes the holes in the p-type emitter to flow towards base (i.e., emitter current  $I_E$ ).

The holes of p-type emitter combine with <sup>electrons of</sup> n-type base. As the base is lightly doped & very thin only few holes (5%) combine with electrons. This causes base current  $I_B$ .

The remaining 95% holes pass over into collector region to constitute collector current  $I_C$ .

$$I_E = I_B + I_C$$

## Transistor Applications

1. Used as an amplifier
2. Switch
3. Oscillator circuit
4. Buffer
5. Logic circuits.

Input is applied between emitter and base, output from Collector and base.

Current amplification factor ( $\alpha$ )

$$\alpha = \frac{I_c}{I_E} \quad \left| \text{constant } V_{CB} \right.$$

\* Ratio of output current to Input current

O/P current  $\rightarrow I_c$  Collector current

I/P current  $\rightarrow I_E$  Emitter current.

\* Current Amplification factor is less than unity

This value can be increased by decreasing base current. This is achieved by making the base thin & doping it lightly

\* Practical values of  $\alpha$  range from 0.9 to 0.99.

Expression for Collector current.

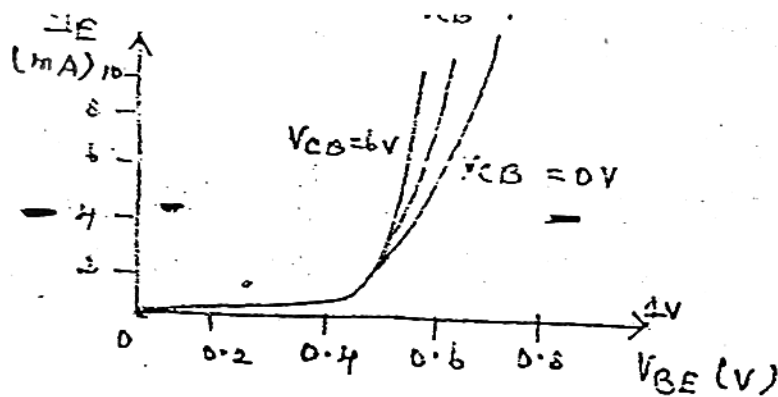
The whole emitter current does not reach Collector a part gives rise to base current

The total Collector current consists of

(i) Part of emitter current which reaches the Collector terminal is  $\alpha I_E$ .

(ii) Leakage current  $I_{\text{leakage}}$  is due to the movement of minority carriers across base Collector junction on reverse biased.

Leakage current smaller than  $I_E$



37  
SM

- (i) The emitter current  $I_E$  increases rapidly with small increase in emitter base voltage  $V_{EB}$  /  $V_{BE}$ . This means input resistance is very small.

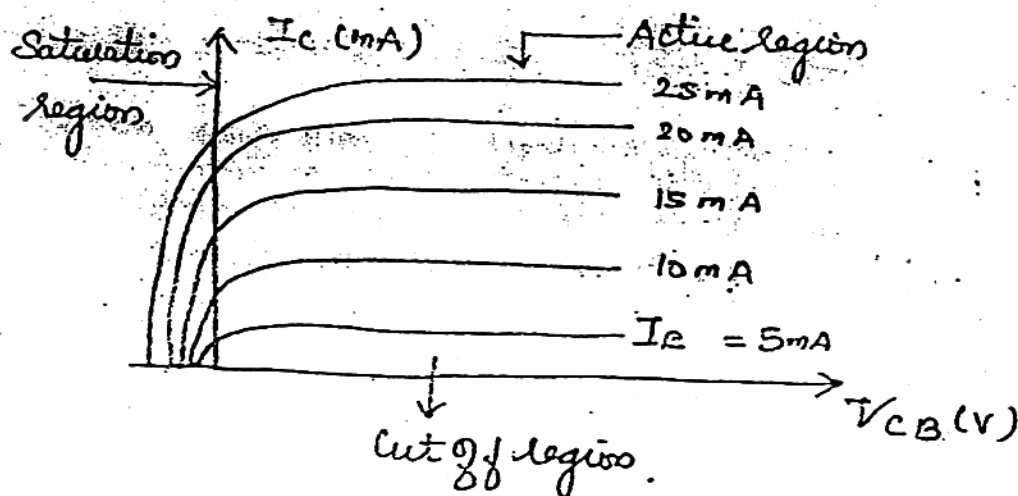
This resistance is known as Dynamic Input resistance

$$r_i = \frac{\Delta V_{EB}}{\Delta I_E} \bigg|_{V_{CB} \text{ constant}}$$

- (ii) emitter current is almost independent of collector voltage

output characteristics

Relates <sup>O/P</sup> collector current ( $I_C$ ) to output voltage, collector to base voltage  $V_{CB}$  at constant input emitter current  $I_E$ .



$$O/P \text{ resistance } r_o = \frac{\Delta V_{CB}}{\Delta I_C} \bigg|_{I_E}$$

## Early effect (or) Base Width Modulation

38  
SM

As the collector Voltage  $V_{CC}$  is made to increase the reverse bias, the depletion width between collector & base tends to increase, with the result that the effective width of the base decreases.

This is known as Base Width modulation

This decrease in effective base width has three consequences.

1.  $\alpha$  Increases with increasing  $V_{CB}$
2. The Charge gradient is increased within the base and consequently, the current of minority carriers injected across the emitter junction increases.
3. For large voltages, the effective base-width may be reduced to zero causing break down in transistor.

Transistor parameters / hybrid parameters / h-parameters

(i) Input Impedance ( $h_{ib}$ )

Ratio of change in emitter voltage to change in emitter current with the collector voltage is kept constant

$$h_{ib} = \left. \frac{\Delta V_{EB}}{\Delta I_E} \right|_{V_{CB} \text{ Constant}}$$

$h_{ib}$  ranges from 20-2 to 50-2.

$$\beta_{d.c.} = h_{FE} = \frac{I_C}{I_B}$$

(6.1.3)

As  $I_C$  is large compared with  $I_{CE0}$ , the large signal current gain ( $\beta$ ) and the d.c. current gain ( $h_{FE}$ ) are approximately equal.

## 6.6 TYPES OF CONFIGURATION

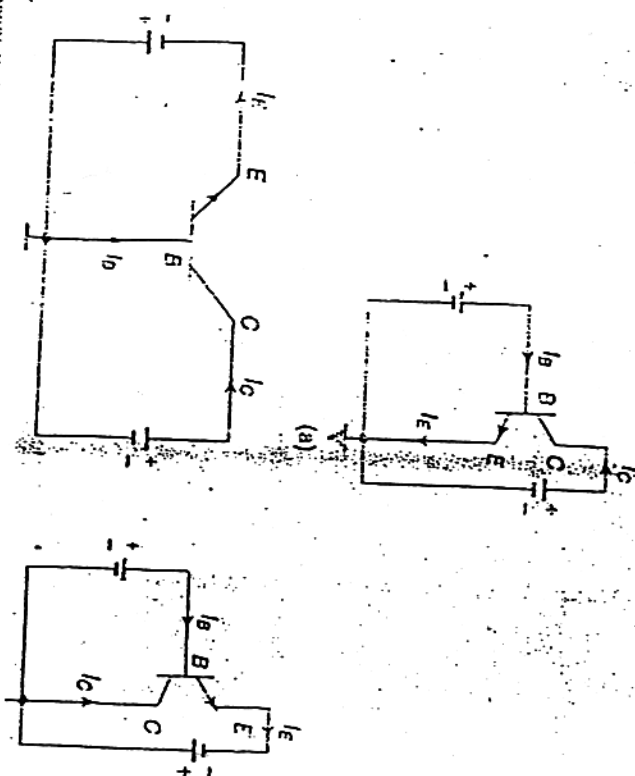
When a transistor is to be connected in a circuit, one terminal is used as an input terminal, the other terminal is used as an output terminal and the third terminal is common to the input and output. Depending upon the input, output and common terminal, a transistor can be connected in three configurations. They are: (i) Common base (CB) configuration, (ii) Common emitter (CE) configuration, and (iii) Common collector (CC) configuration.

(i) **CB configuration** This is also called grounded base configuration. In this configuration, emitter is the input terminal, collector is the output terminal and base is the common terminal.

(ii) **CE configuration** This is also called grounded emitter configuration. In this configuration, base is the input terminal, collector is the output terminal and emitter is the common terminal.

(iii) **CC configuration** This is also called grounded collector configuration. In this configuration, base is the input terminal, emitter is the output terminal and collector is the common terminal.

The supply voltage connections for normal operation of an NPN transistor in the three configurations are shown in Fig. 6.6.



## 6.6.1 CB Configuration

The circuit diagram for determining the static characteristics curves of an NPN transistor in the common base configuration is shown in Fig. 6.7.

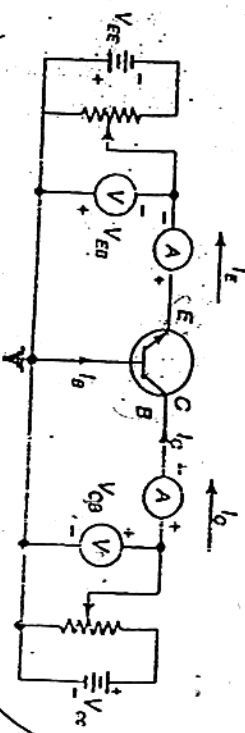


Fig. 6.7 Circuit to determine CB static characteristics

**Input characteristics** To determine the input characteristics, the collector-base voltage  $V_{CB}$  is kept constant at zero volt and the emitter current  $I_E$  is increased from zero in suitable equal steps by increasing  $V_{EE}$ . This is repeated for higher fixed values of  $V_{CB}$ . A curve is drawn between emitter current  $I_E$  and emitter-base voltage  $V_{EB}$  at constant collector-base voltage  $V_{CB}$ . The input characteristics thus obtained are shown in Fig. 6.8.

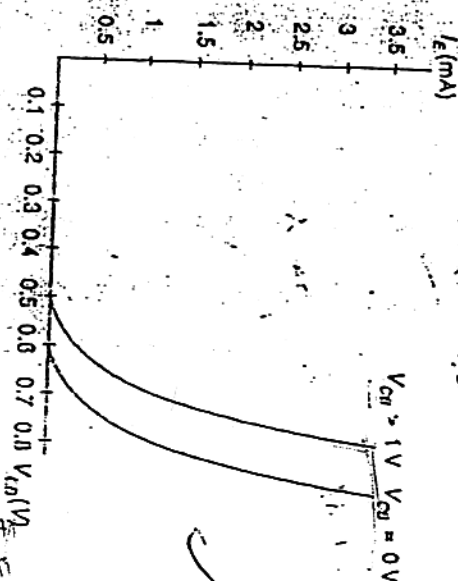


Fig. 6.8 CB input characteristics

When  $V_{CB}$  is equal to zero and the emitter-base junction is forward biased as shown in the characteristics, the junction behaves as a forward biased diode so that emitter current  $I_E$  increases rapidly with small increase in emitter-base voltage  $V_{EB}$ . When  $V_{CB}$  is increased keeping  $V_{EB}$  constant, the width of the base region will decrease. This effect results in an increase of  $I_E$ . Therefore, the curves shift towards the left as  $V_{CB}$  is increased.

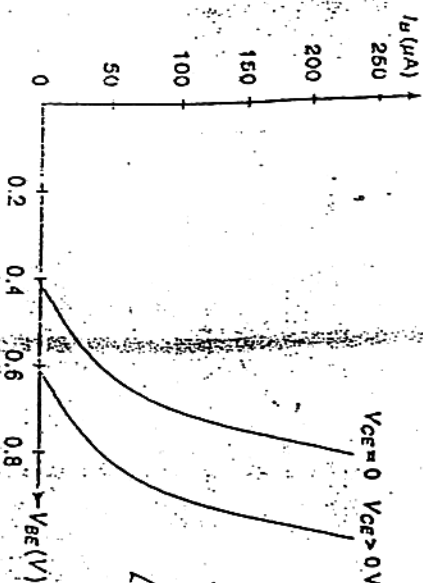


Fig. 6.11 CE input characteristics

When  $V_{CE} = 0$ , the emitter-base junction is forward biased and the junction behaves as a forward biased diode. Hence, the input characteristic for  $V_{CE} = 0$  is similar to that of a forward-biased diode. When  $V_{CE}$  is increased, the width of the depletion region at the reverse biased collector-base junction will increase. Hence the effective width of the base will decrease. This effect causes a decrease in the base current  $I_B$ . Hence, to get the same value of  $I_B$  as that for  $V_{CE} = 0$ ,  $V_{BE}$  should be increased. Therefore, the curve shifts to the right as  $V_{CE}$  increases.

**Output characteristics.** To determine the output characteristics, the base current  $I_B$  is kept constant at a suitable value by adjusting base-emitter voltage,  $V_{BE}$ . The magnitude of collector-emitter voltage  $V_{CE}$  is increased in suitable equal steps from zero and the collector current  $I_C$  is noted for each setting  $V_{CE}$ . Now the curves of  $I_C$  versus  $V_{CE}$  are plotted for different constant values of  $I_B$ . The output characteristics thus obtained are shown in Fig. 6.12. From Eqs. (6.6) and (6.7), we have

$$\beta = \frac{\alpha}{1 - \alpha} \quad \text{and} \quad I_C = (1 + \beta) I_{EBO} + \beta I_B$$

For larger values of  $V_{CE}$ , due to Early effect, a very small change in  $\alpha$  is reflected in a very large change in  $\beta$ . For example, when  $\alpha = 0.98$ ,  $\beta = \frac{0.98}{1 - 0.98} = 49$ . If  $\alpha$  increases to 0.985, then  $\beta = \frac{0.985}{1 - 0.985} = 66$ . Here, a slight increase in  $\alpha$  by about 0.5% results in an increase in  $\beta$  by about 34%. Hence, the output characteristics of

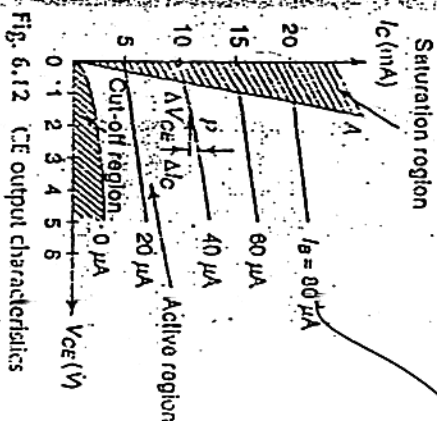


Fig. 6.12 CE output characteristics

**saturation region** (hatched), and the line OA is called the saturation line. In this region, both junctions are forward biased and an increase in the base current does not cause a corresponding large change in  $I_C$ . The ratio of  $V_{CE(sat)}$  to  $I_C$  in this region is called saturation resistance.

The region below the curve for  $I_B = 0$  is called the **cut-off region** (hatched). In this region, both junctions are reverse biased. When the operating point for the transistor enters the cut-off region, the transistor is OFF. Hence, the collector current becomes almost zero and the collector voltage almost equals  $V_{CC}$ , the collector supply voltage. The transistor is virtually an open circuit between collector and emitter.

The central region where the curves are uniform in spacing and slope is called the **active region** (unhatched). In this region, emitter-base junction is forward biased and the collector-base junction is reverse biased. If the transistor is to be used as a linear amplifier, it should be operated in the active region.

If the base current is subsequently driven large and positive, the transistor switches into the saturation region via the active region, which is traversed at a rate that is dependent on factors such as gain and frequency response. In this ON condition, large collector current flows and collector voltage falls to a very low value, called  $V_{CE(sat)}$ , typically around 0.2 V for a silicon transistor. The transistor is virtually a short circuit in this state.

High-speed switching circuits are designed in such a way that transistors are not allowed to saturate, thus reducing switching times between ON and OFF times.

**Transistor parameters** The slope of the CE characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common emitter hybrid parameters or *h-parameters*.

(i) **Input impedance ( $h_{ie}$ ):** It is defined as the ratio of the change in (input) base voltage to the change in (input) base current with the (output) collector voltage  $V_{CE}$  kept constant. Therefore,

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}, \quad V_{CE} \text{ constant} \quad (6.18)$$

It is the slope of CE input characteristics  $I_B$  versus  $V_{BE}$  as shown in Fig. 6.11. The typical value of  $h_{ie}$  ranges from 500 to 2000  $\Omega$ .

(ii) **Output admittance ( $h_{oe}$ ):** It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage with the (input) base current  $I_B$  kept constant. Therefore,

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}, \quad I_B \text{ constant} \quad (6.19)$$

It is the slope of CE output characteristic  $I_C$  versus  $V_{CE}$  as shown in Fig. 6.12. The typical value of this parameter is of the order of 0.1 to 10  $\mu\text{mhos}$ .

(iii) **Forward current gain ( $h_{fe}$ ):** It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) base current keeping the (output) collector voltage  $V_{CE}$  constant. Hence,

The process of raising the strength of a weak signal without any change in its shape is known as Amplification.

To ensure proper amplification, the following basic conditions must be satisfied.

- \* Proper Zero Signal collector current

- \* Minimum proper base-emitter Voltage  $V_{BE}$  at any instant

- \* Minimum proper Collector-emitter Voltage  $V_{CE}$  at any instant

Condition 1 & 2 ensures that emitter-base junction is forward biased

Condition 3 ensures that Collector-base junction is reverse biased.

∴ Transistor is in Active region.

### Transistor biasing

The proper flow of Zero Signal collector current and maintenance of proper collector-emitter Voltage during the passage of signals is called Transistor Biasing.

Biasing can be achieved with a bias battery or associating a circuit with a transistor. The circuit which provides proper biasing for a transistor is called Biasing circuit.

$$1 - \beta \frac{\partial I_B}{\partial I_C} = \frac{1 + \beta}{S}$$

$$S = \frac{1 + \beta}{1 - \beta \left( \frac{\partial I_B}{\partial I_C} \right)}$$

$\therefore S$  should be small to have better thermal runaway.

Stability factor  $S'$

Defined as the rate of change of  $I_C$  w.r.t  $V_{BE}$ ,  
 keeping  $I_{CO}$ ,  $\beta$  constant

$$S' = \frac{\partial I_C}{\partial V_{BE}} \bigg|_{\beta, I_{CO} \text{ constant}}$$

Stability factor  $S''$

Defined as the rate of change of  $I_C$  w.r.t  $\beta$ ,  
 keeping  $I_{CO}$ ,  $V_{BE}$  constant

$$S'' = \frac{\partial I_C}{\partial \beta} \bigg|_{V_{BE}, I_{CO} \text{ constant}}$$

### Methods of Transistor Biasing

The following are the most commonly used methods of obtaining transistor biasing from one source of supply i.e.,  $V_{CC}$ .



To find stability factor  $S$ :

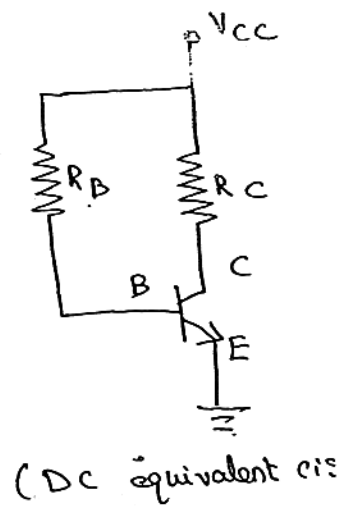
& Apply KVL to the base we get.

$$V_{CC} = I_B R_B + V_{BE} \quad \dots (1)$$

$$V_{CC} - V_{BE} = I_B R_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \dots (2)$$

w.k.t  $S = \frac{1 + \beta}{1 + \beta \left( \frac{dI_B}{dI_C} \right)} \quad \dots (3)$



$\therefore$  differentiate equ (2) w.r.t  $I_C$  we get

$$\frac{dI_B}{dI_C} = 0; \text{ substitute } \frac{dI_B}{dI_C} \text{ in equ (3) we get}$$

$$S = \frac{1 + \beta}{1 + \beta(0)} = 1 + \beta //$$

$$\beta = \frac{I_C}{I_B}$$

To find stability factor  $S'$ :  $S' = \frac{\partial I_C}{\partial V_{BE}}$

$$S' = \beta \frac{dI_B}{dV_{BE}} \quad \dots (4)$$

$\therefore$  differentiate equ (2) w.r.t  $V_{BE}$  we get.

$$\frac{dI_B}{dV_{BE}} = \frac{d}{dV_{BE}} \left[ \frac{V_{CC}}{R_B} - \frac{V_{BE}}{R_B} \right] = -\frac{1}{R_B}$$

Substitute  $\frac{dI_B}{dV_{BE}}$  in equ (4) we get.

$$S' = \beta \cdot \left( -\frac{1}{R_B} \right) = -\frac{\beta}{R_B}$$

$$V_{CC} = I_B [R_C + R_B] + V_{BE} + I_C R_C \quad \dots (2)$$

w.k.t  $\beta = \frac{I_C}{I_B} \Rightarrow I_C = \beta I_B$

$$\therefore V_{CC} = I_B [R_C + R_B] + V_{BE} + \beta I_B R_C$$

$$V_{CC} = I_B [(1 + \beta) R_C + R_B] + V_{BE} \quad \dots (3)$$

$$V_{CC} - V_{BE} = I_B [(1 + \beta) R_C + R_B]$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{[(1 + \beta) R_C + R_B]} \quad \dots (4)$$

To find S:-

consider equ (2) and differentiate equ (2)

w.r.t  $I_C$  we get

$$0 = \frac{dI_B}{dI_C} [R_C + R_B] + 0 + R_C$$

$$-R_C = \frac{dI_B}{dI_C} [R_C + R_B]$$

$$\therefore \frac{dI_B}{dI_C} = \frac{-R_C}{[R_C + R_B]} \quad \dots (5)$$

w.k.t.

$$S = \frac{1 + \beta}{1 + \beta \cdot \frac{dI_B}{dI_C}}$$

Sub (5) in S we get.

$$S = \frac{1 + \beta}{1 + \beta \left[ \frac{R_C}{R_C + R_B} \right]} \quad \dots (6)$$

$$S'' = \frac{(V_{CC} - V_{BE}) (R_C + R_B)}{[(1 + \beta) R_C + R_B]^2} \quad (0.9) \quad \frac{I_C}{\beta} \quad \frac{S}{(1 + \beta)}$$

## Voltage divider Bias:

In voltage divider bias circuit, the biasing is provided by three resistors  $R_1$ ,  $R_2$  and  $R_E$ .

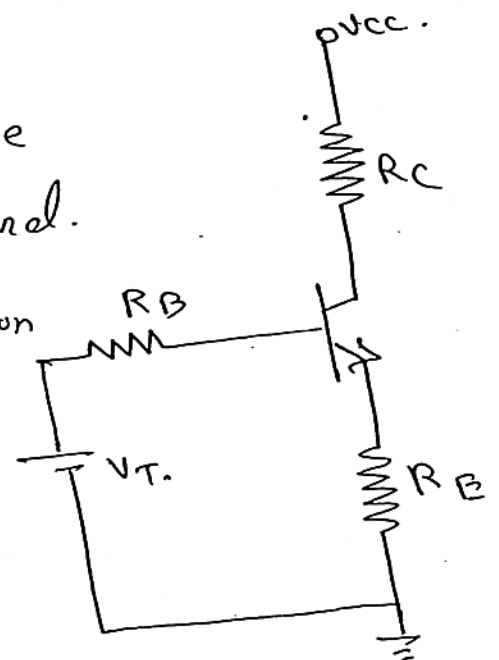
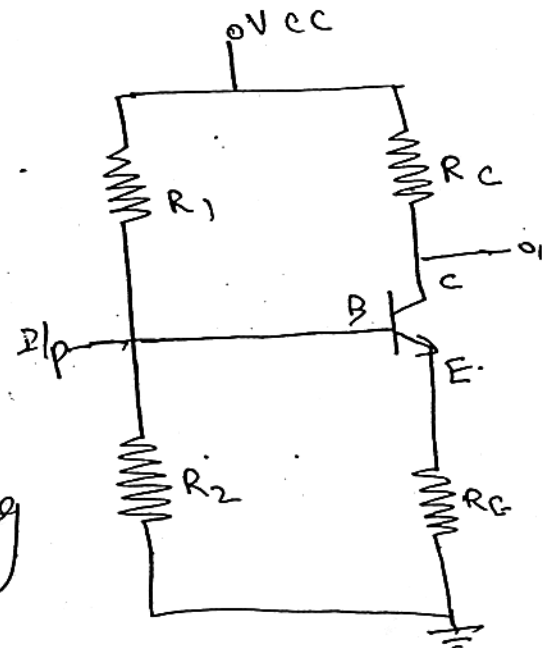
The resistors  $R_1$  and  $R_2$  act as a potential divider giving a fixed voltage.

The Thevenin's equivalent

circuit of voltage divider bias. Here  $R_1$  and  $R_2$  are replaced by  $R_B$  and  $V_T$  where  $R_B$  is parallel combination of  $R_1$  and  $R_2$  and  $V_T$  is Thevenin voltage.

$$V_T = V_{CC} \cdot \frac{R_2}{R_1 + R_2} \quad \text{and}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$



(Thevenin equivalent)

To find  $S'$ :

Consider expression for  $V_T$

$$V_T = (R_B + R_E) I_B + I_C R_E + V_{BE} \quad \text{--- (6)}$$

w.k.t  $I_C = \beta I_B + (1 + \beta) I_{CO}$

$$I_C - (1 + \beta) I_{CO} = \beta I_B$$

$$I_B = \frac{I_C}{\beta} - \frac{(1 + \beta)}{\beta} I_{CO} \quad \text{--- (7)}$$

Sub equ (7) in (6) we get.

$$V_T = (R_B + R_E) \left[ \frac{I_C}{\beta} - \frac{(1 + \beta)}{\beta} I_{CO} \right] + I_C R_E + V_{BE}$$

$$V_T = (R_B + R_E) \frac{I_C}{\beta} - \frac{(1 + \beta)}{\beta} I_{CO} (R_B + R_E) + I_C R_E + V_{BE} \quad \text{--- (8)}$$

diff above equation w.r.t  $V_{BE}$  we get

$$0 = \frac{(R_B + R_E)}{\beta} \frac{dI_C}{dV_{BE}} + R_E \frac{dI_C}{dV_{BE}} + 1$$

$$-1 = \left[ \frac{R_B + (1 + \beta) R_E}{\beta} \right] \frac{dI_C}{dV_{BE}}$$

$$\therefore S' = \frac{dI_C}{dV_{BE}} = \frac{-\beta}{R_B + (1 + \beta) R_E} \quad \text{U.} \quad \text{--- (9)}$$

To find  $S''$ :

$$S'' = \frac{dI_C}{d\beta}$$

$$\therefore \frac{dI_C}{d\beta} = \left[ V_T - V_{BE} + I_{CO}(R_B + R_E) \right] \cdot \frac{\left[ (R_B + (1+\beta)R_E) - \beta(R_E) \right]}{\left[ R_B + (1+\beta)R_E \right]^2}$$

$$= \frac{\left[ V_T - V_{BE} + I_{CO}(R_B + R_E) \right] \left[ R_B + R_E + \cancel{\beta R_E} - \cancel{\beta R_E} \right]}{\left[ R_B + (1+\beta)R_E \right]^2}$$

$$= \frac{\left[ V_T - V_{BE} + I_{CO}(R_B + R_E) \right] (R_B + R_E)}{\left[ R_B + (1+\beta)R_E \right]^2}$$

$$S'' = \frac{dI_C}{d\beta} = \frac{(R_B + R_E)}{\left[ R_B + (1+\beta)R_E \right]} \cdot \frac{\left[ V_T - V_{BE} + I_{CO}(R_B + R_E) \right]}{\left[ R_B + (1+\beta)R_E \right]}$$

$$S'' = \frac{R_B + R_E}{\left[ R_B + (1+\beta)R_E \right]} \cdot \frac{I_C}{\beta} \quad (O.S.)$$

$$S'' = \frac{I_C S}{\beta(1+\beta)}$$

## Field effect transistor (FET)

FET is a unipolar (depending on either electron (n-channel) or hole (p-channel) conduction), three terminal device

\* Voltage controlled device

ie., the output current is controlled by the electric field created by the applied potential to the control terminal.

\* High Input Impedance device

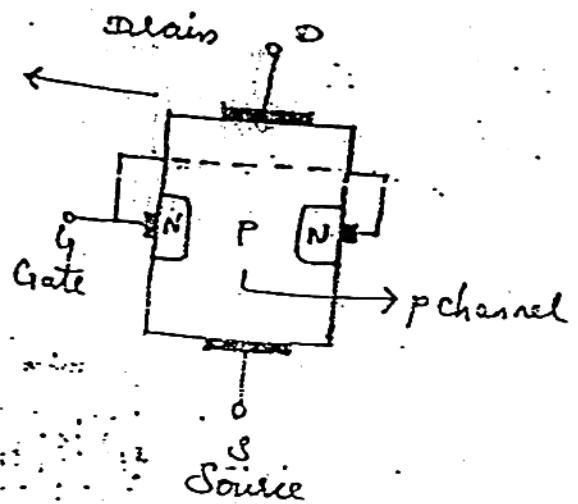
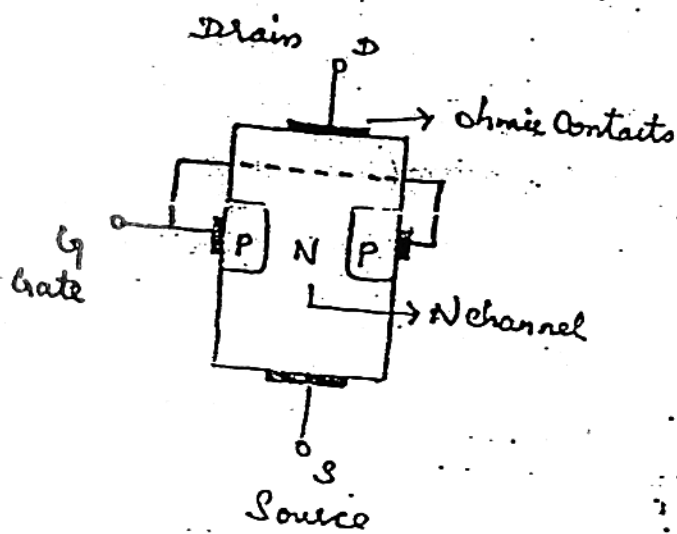
### Construction

FET consists of a P-type or N-type semiconductor with two PN junctions.

The space between the junctions is called channel.

\* If bar is N-type, then channel is N-channel FET

\* If bar is P-type, then channel is P-channel FET



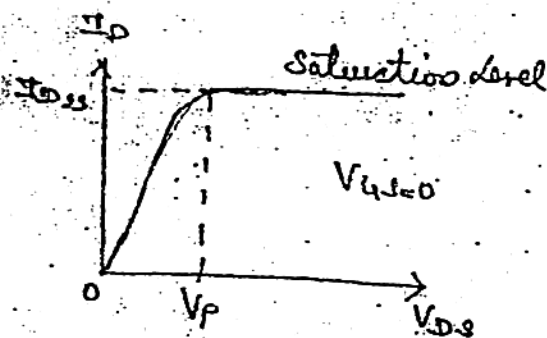
When a voltage  $V_{DS}$  is applied between drain & source terminals and voltage on gate is zero, the two PN junctions at the sides of the bar establish depletion layers.

The electrons flow from source to drain through channel. The size of the depletion layer determines the width of the channel and hence the current conduction through the bar.

If  $V_{DS}$  is ~~increased~~ <sup>minimised</sup>, at a certain level the depletion regions would touch, which results in pinch off condition.

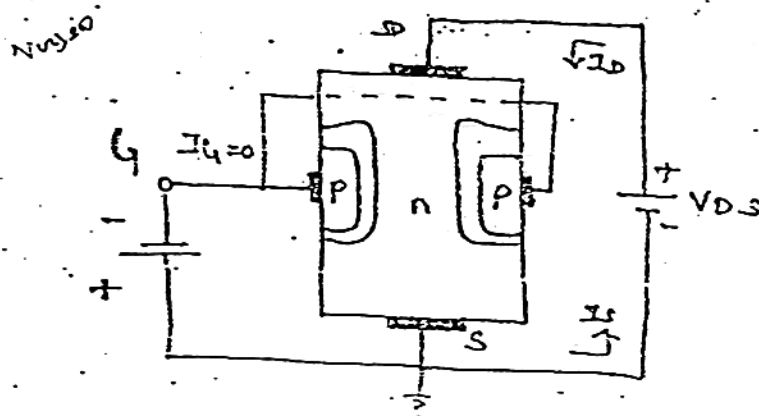
The level of  $V_{DS}$  that establishes this condition is referred to as pinch off voltage ( $V_p$ ).

The high electric field prevents the depletion regions from meeting, hence current saturates i.e., for further increase in  $V_{DS}$ , the  $I_D$  remains constant. This region is called pinch off region.



(ii)  $V_{GS} = -V_e$

$V_{DS} \neq 0$  (Some positive)



cut off region

$$I_D = 0, \quad V_{GS} > V_{GS(Off)}$$

With increase in negative  $V_{GS}$ , the channel width available for conduction decreases. At certain voltage  $V_{GS(Off)}$ , depletion region touches each other & closes the channel completely.

Saturation region

Region where  $I_D$  remains constant for different values of  $V_{DS}$ .

Ohmic region

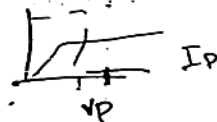
$I_D$  varies with variation in drain to source voltage  $V_{DS}$ . JFET operates as a voltage variable resistance in Ohmic region.

Breakdown region

If value of  $V_{DS}$  increased beyond pinch off voltage  $V_P$  the drain current  $I_D$  remains constant.

If  $V_{DS}$  further increased the gate-channel junction breaks due to avalanche effect. At this point drain current  $I_D$  increases very rapidly & the device may be destroyed.

Parameters of JFET

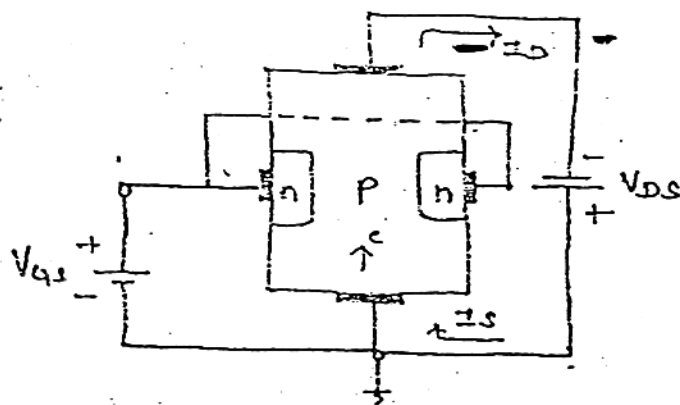


\* Mutual conductance ( $\mu$ ) transconductance ( $g_m$ )

$$g_m = \left( \frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS}} = \frac{\Delta I_D}{\Delta V_{GS}} \Big|_{V_{DS} = \text{Constant}}$$



## P-Channel JFET



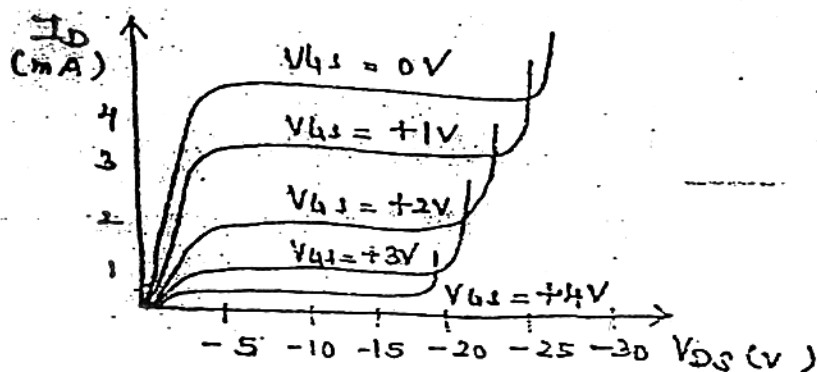
The p-channel JFET is constructed in same manner as n-channel but with p-type & n-type materials reversed.

The Current directions are reversed and also Voltage polarities are reversed.

Drain Current increases with increase in negative  $V_{DS}$  Vol

Gate to Source Voltage  $V_{GS}$  is positive and the drain current decreases with increasing  $V_{GS}$  Voltage.

Drain Characteristics of P-Channel JFET.



## Comparison

### JFET

#### 1. Unipolar device

- \* Operation depends on flow of Majority carriers  
ie., holes for P channel  
& electrons for N channel

FETs

#### 2. Voltage controlled device

- \* Voltage I/p controls current output

#### 3. Less Noise

#### 4. High Input Impedance

#### 5. Low output Impedance

#### 6. High power gain

#### 7. No thermal runaway

#### 8. High Switching Speed

#### 9. Source & Drain terminals are interchangeable

### BJT

#### Bipolar device

- \* Operation depends on both majority & minority carriers.

#### Current Controlled device

- \* Current I/p controls current output.

#### More Noise

#### Low Input Impedance

#### High output Impedance

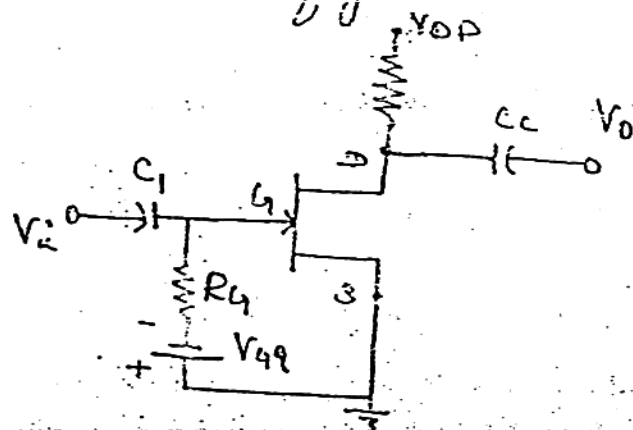
#### Low power gain

#### Thermal runaway occurs

#### Lower Switching Speed

#### Emitter & collector terminals are not interchangeable.

## \* Fixed Bias Configuration



n-channel JFET

- The Coupling Capacitors are open circuits for DC Analysis or Short circuit (low Impedance) for AC Analysis.

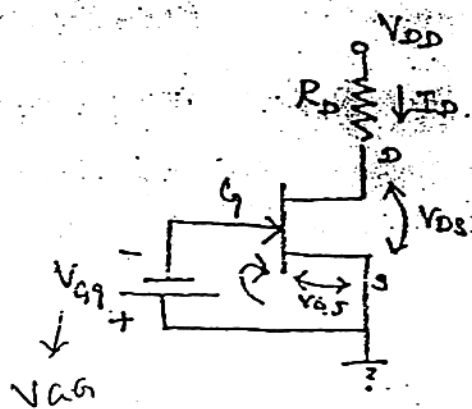
Resistor  $R_G$  is present to ensure that  $V_i$  appears at the Input to FET. for AC Analysis.

For DC Analysis

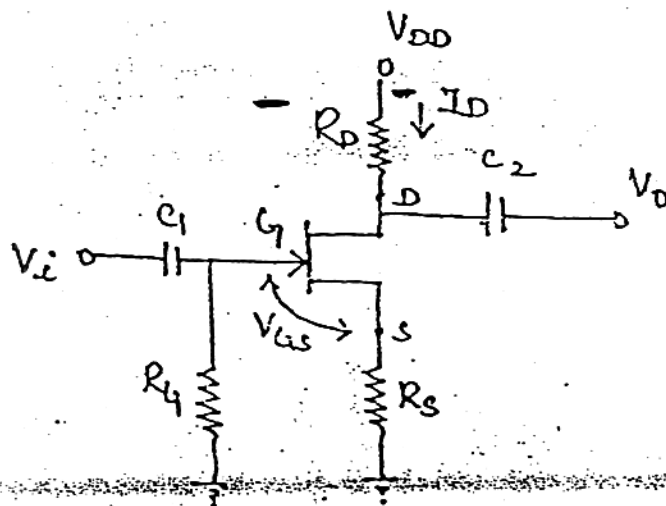
$$I_G \approx 0$$

$$V_{R_G} = I_G R_G = 0V$$

- The Zero Volt drop across  $R_G$  permits replacing  $R_G$  by a Short circuit equivalent



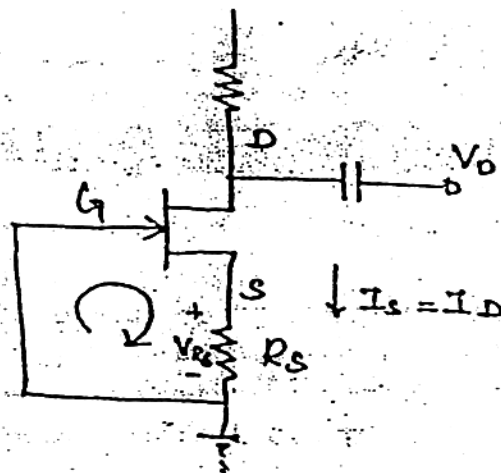
## Self bias Configuration



Self bias Configuration eliminates the need for two dc supplies. The Controlling Voltage  $V_{GS}$  is determined by  $\frac{R_2}{R_1 + R_2} V_{DD}$ .

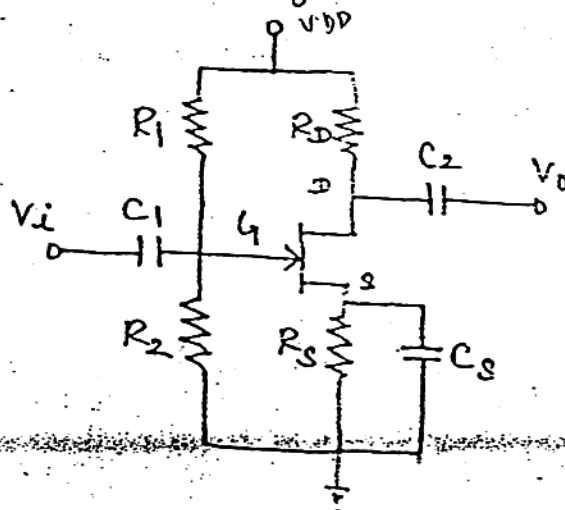
For D.C Analysis,

Capacitors are replaced by open circuits.  
 $R_1$  replaced by short circuit.



The current through  $R_S$  is source current  $I_S$ , but  $I_S = I_D$   
 and  $V_{RS} = I_S R_S$   
 (or)  
 $= I_D R_S$ .

## Voltage divider biasing



Network redrawn for dc analysis by open circuiting, All the capacitors ( $C_1, C_2, C_S$ ).

The Voltage  $V_G$  across  $R_2$  can be found using Voltage divider bias

$$V_G = \frac{R_2}{R_1 + R_2} \cdot V_{DD}$$

Applying KVL

$$V_G - V_{GS} - V_{RS} = 0$$

$$\therefore V_{GS} = V_G - V_{RS}$$

Substituting  $V_{RS} = I_S R_S$

(or)

$$V_{RS} = I_D R_S$$

$$\therefore \boxed{V_{GS} = V_G - I_D R_S}$$

Applying KVL to output circuit

$$V_{DD} - V_{DS} - I_D R_D - I_S R_S = 0$$

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$\boxed{I_S = I_D}$$

## MOSFET

\* Metal Oxide Semiconductor Field Effect Transistor

\* Types of MOSFET

1. Enhancement MOSFET

2. Depletion MOSFET

\* Principle (Working)

By Applying electric field across insulator the thickness and Resistance of Conducting channel of semiconductor material can be controlled.

In Depletion MOSFET,

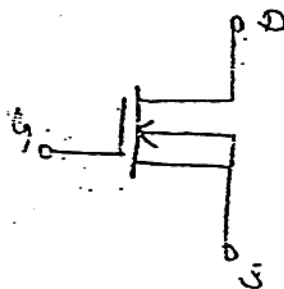
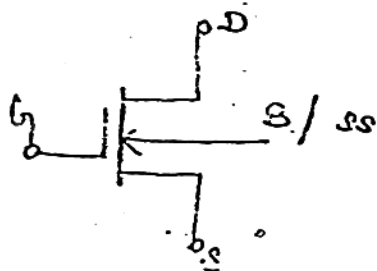
The controlling electric field reduces the number of minority carriers available for conduction.

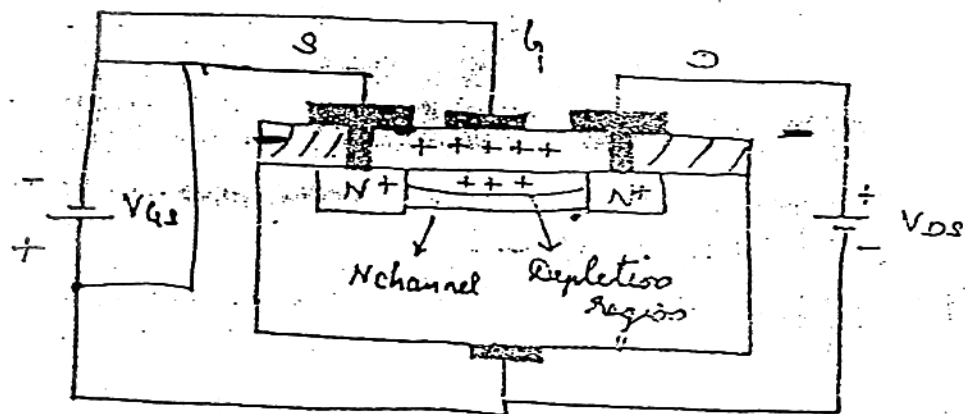
In Enhancement MOSFET,

The controlling electric field increases the Majority carriers available for conduction.

\* N-Channel Depletion MOSFET

Symbol

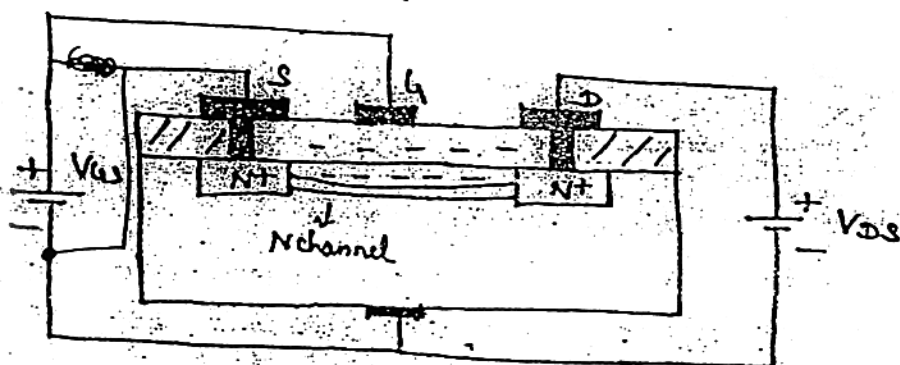




The negative voltage on gate induces positive charge in the ch. Because of this free electrons are repelled away in the channel. As a result the channel is depleted of electrons hence named depletion mode.

—  $V_{GS}$ , increases, the drain current  $I_D$  decreases

Enhancement mode

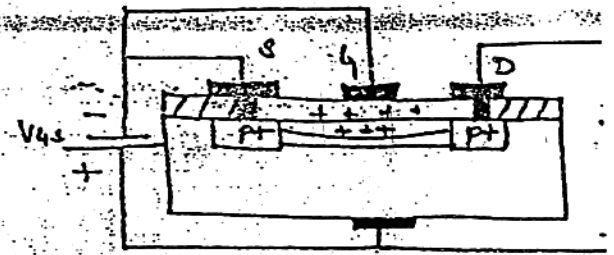
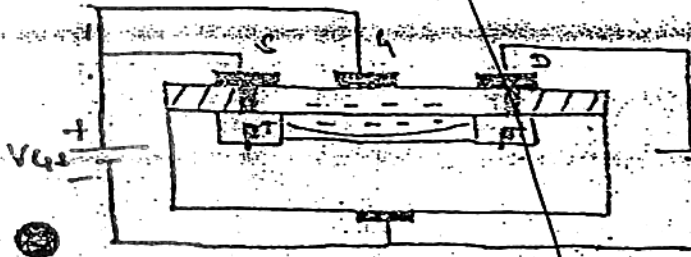
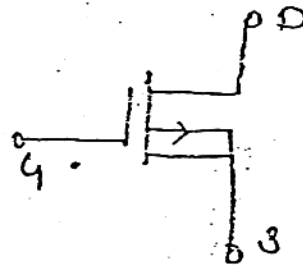
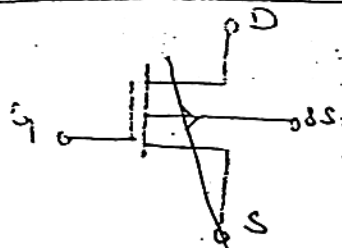


In this mode, both the gate & drain are maintained at positive potential w.r.t Source.

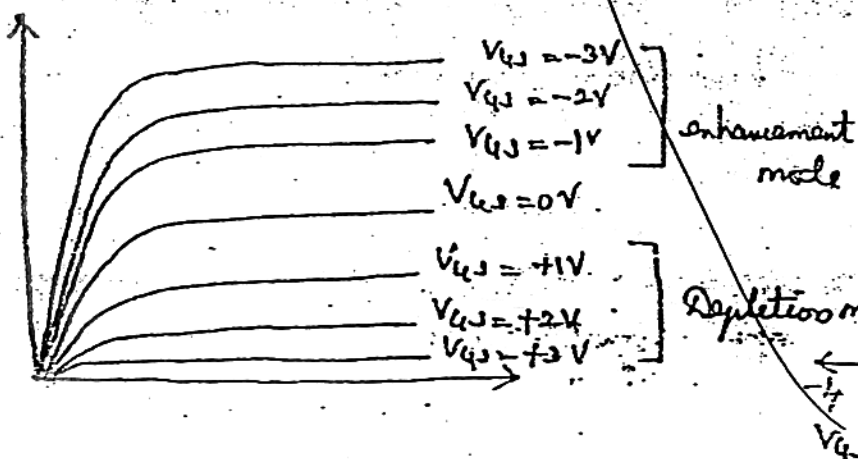
The positive voltage on gate induces negative charge in the channel. Hence named enhancement mode.

+  $V_{GS}$  Increases, the drain current  $I_D$  increases

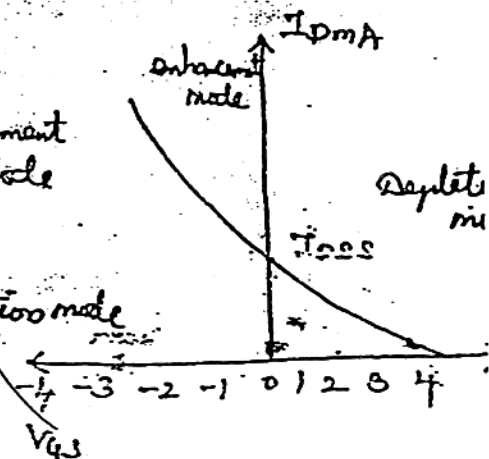
# \* P-Channel Depletion MOSFET



## Drain Characteristics



## Transfer Characteristics





## N channel Enhancement

Three modes of operation are available.

\* Accumulation

\* Depletion

\* Inversion

\* Accumulation :- ( $V_{GS}$  is negative)

If a negative voltage is applied at the gate terminal. The majority carriers (holes) from the p-type substrate are attracted towards the gate terminal. The charge carriers are accumulated underneath the gate oxide layer.

\* Depletion :- ( $V_{GS}$  is small positive)

If a small positive is applied the holes will be repelled into the substrate. The repelled holes move to the substrate and create negatively charged fixed acceptor ions under the gate oxide layer.

N channel enhancement MOSFET operates with positive gate to Source Voltage  $V_{GS}$  and positive  $V_{DS}$ .

(i) When  $V_{GS} = 0$

Device is reverse biased

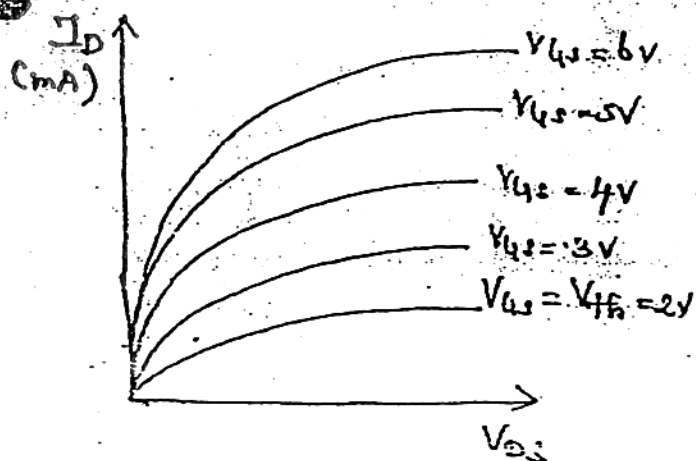
(ii) When  $V_{GS} = +ve$  Voltage, negative charges are induced in the Substrate.

This induced charges form the inversion layer between Source (S) and Drain (D).

The inversion layer is formed if  $V_{GS}$  exceeds  $V_{th}$  which increases drain current  $I_D$ .

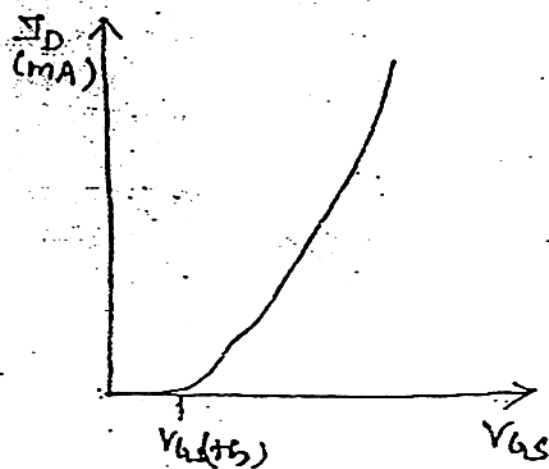
Drain current is enhanced by  $+V_{GS}$  and hence this device is called enhancement type MOSFET.

Drain Characteristics



The curve drawn between drain current ( $I_D$ ) and drain to source voltage ( $V_{DS}$ ).

Transfer Characteristics



The curve drawn between drain current and  $V_{GS}$ . The voltage reaches  $V_{th}$ . That time

## MOSFET BIASING

### \* Biasing of Depletion-type MOSFET

The similarities in appearance between the transfer curves JFET & Depletion-type MOSFETs permit a similar analysis in the dc domain.

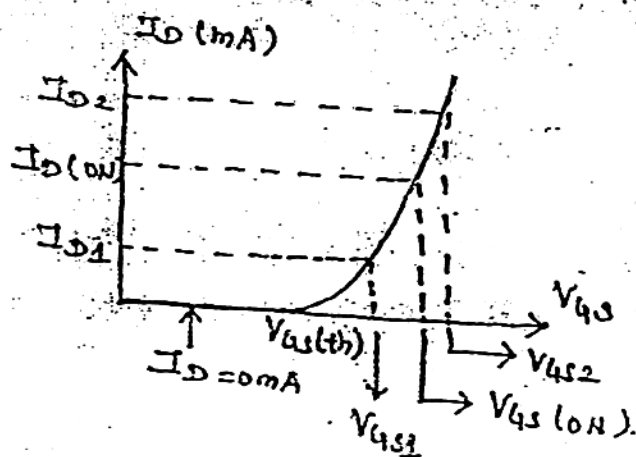
The difference is in depletion type MOSFET, the operating points have positive values of  $V_{GS}$  and  $I_D$  exceeds  $I_{DSS}$ .

The analysis is same for D-MOSFET like JFET.

### \* Biasing of enhancement-type MOSFET

The transfer characteristics of enhancement-type MOSFET are different from JFET & depletion-type MOSFET.

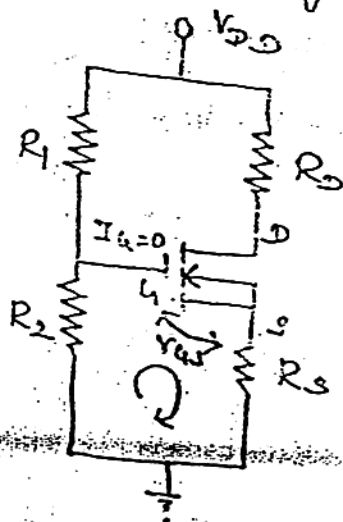
For n-channel enhancement type MOSFET, the drain current is zero for  $V_{GS}$  less than  $V_{GS(th)}$ .



For levels of  $V_{GS}$  greater than  $V_{GS(th)}$ , the drain current is defined by

$$I_D = k (V_{GS} - V_{GS(th)})^2$$

## 2. Voltage divider biasing



Voltage divider Rule

$$V_G = \frac{R_2}{R_1 + R_2} \cdot V_{DD}$$

Applying KVL (I/P)

$$+V_G - V_{GS} - V_{RS} = 0$$

and  $V_{GS} = V_G - V_{RS}$

(or)

$$V_{GS} = V_G - I_D R_S$$

Applying KVL (O/P)

$$V_{DD} - V_{RD} - V_{DS} - V_{RS} = 0$$

and  $V_{DS} = V_{DD} - V_{RS} - V_{RD}$

$$V_{DS} = V_{DD} - I_D R_S - I_D R_D$$

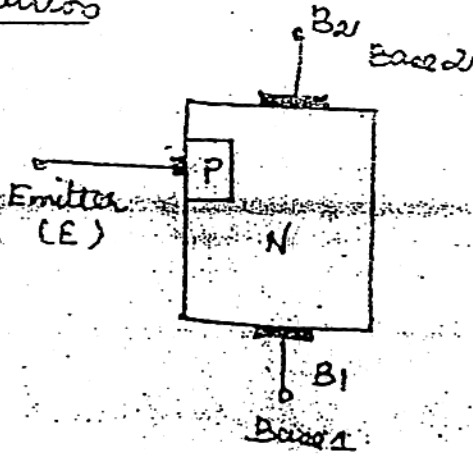
$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$

## UNI Junction Transistor (UJT)

45  
SM

Single junction (like ordinary PN junction diode) on three terminal Semiconductor device

### Construction



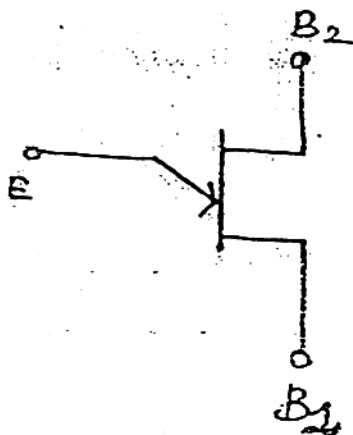
Consists of N-type Silicon bar and P-type Silicon regions.

- \* N-type bar acts as base region
- \* P-type bar acts as emitter region

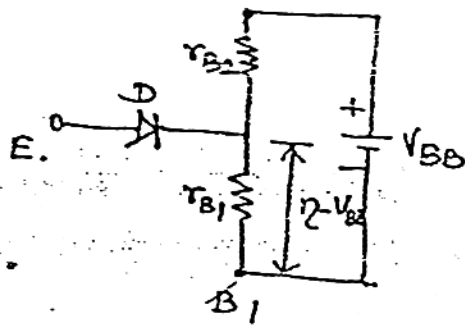
P N junction formed between base and emitter regions.

The emitter region is heavily doped, while the base region is lightly doped. Hence the resistivity of the base material is high.

### Symbol



Emitter (E)  
Base 1 (B1)  
Base 2 (B2)



As emitter is open, applied voltage divides itself across resistance  $r_{B1}$  and  $r_{B2}$ .

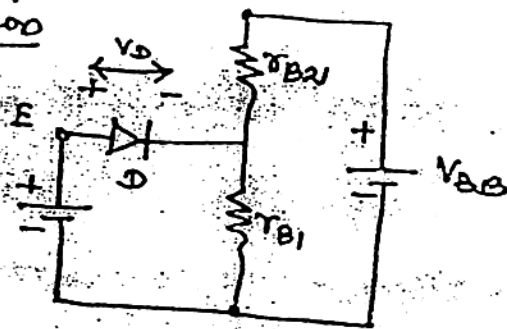
Voltage across the resistance  $r_{B1}$  is

$$V_1 = \frac{r_{B1}}{r_{B1} + r_{B2}} \times V_{BB}$$

$$V_1 = \frac{r_{B1}}{r_{BB}} \times V_{BB}$$

The voltage drop across the resistance  $r_{B1}$  is called the intrinsic stand off voltage.

operation



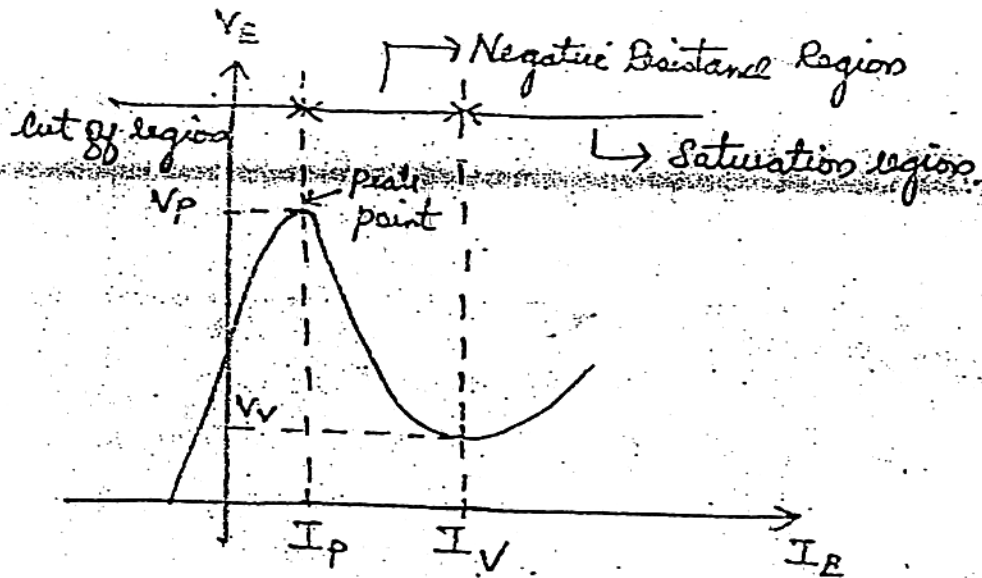
Emitter diode D is reverse biased by a voltage drop across the resistance  $r_{B1}$  ( $\eta \cdot V_{BB}$ ) and  $V_D$ .

$\therefore$  Total reverse bias voltage across diode is sum of  $\eta V_{BB}$  and  $V_D$ . (This reverse biases the PN junction & emitter current is cut off).

If a negative Voltage is applied to emitter, PN junctions become reverse biased and the emitter current is cut off.

UJT is in OFF state.

### V-I Characteristics



Peak point and Valley point divide the curve into three important regions.

#### \* Cut off region

emitter voltage is below peak point voltage  $V_p$ , the emitter current is zero.

UJT is OFF (cut off).

#### \* Negative resistance Region

Region between the peak point and valley point is called negative resistance region.

emitter voltage decreases from  $V_p$  to  $V_v$   
emitter current increases from  $I_p$  to  $I_v$ .

Use:-  
(purpose)

48

51

Relation oscillator using UJT is used to generate Quasi square wave form.

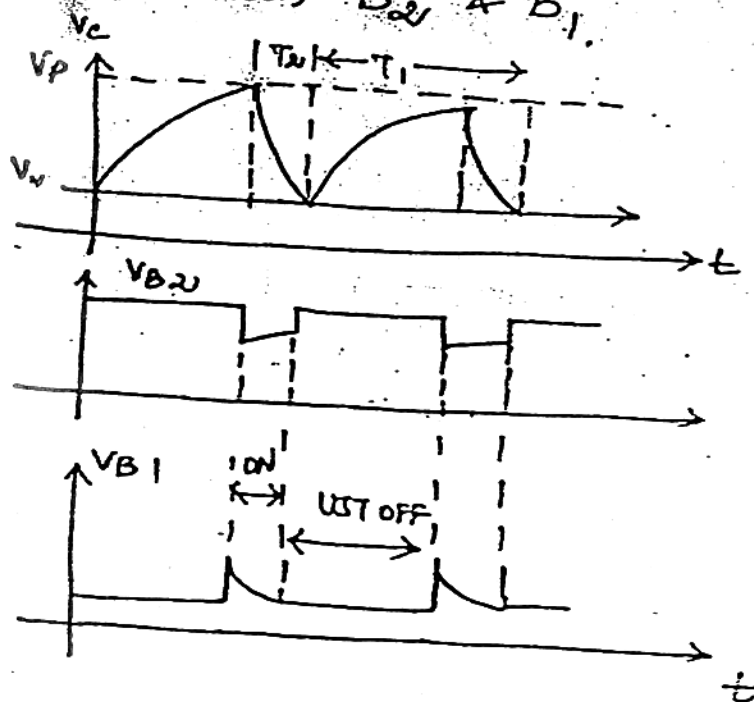
It consists of UJT and a capacitor  $C$  which is charged through  $R$  as the supply voltage  $V_{BB}$  is switched ON.

Voltage across the capacitor increases exponentially and when the capacitor voltage reaches peak point voltage  $V_p$ , UJT starts conducting and the capacitor voltage is discharged through  $E B_1$  and  $R_1$ .

After peak point, it provides negative resistance to the discharge path.

As capacitor voltage reaches zero, device turns off capacitor  $C$  charge again. produces continuous waveforms

Spikes produced by the inclusion of resistances  $R_2$  &  $R_1$  in series with  $B_2$  &  $B_1$ .





# Thyristor

495

four layer PNPN device, which has three PN junctions

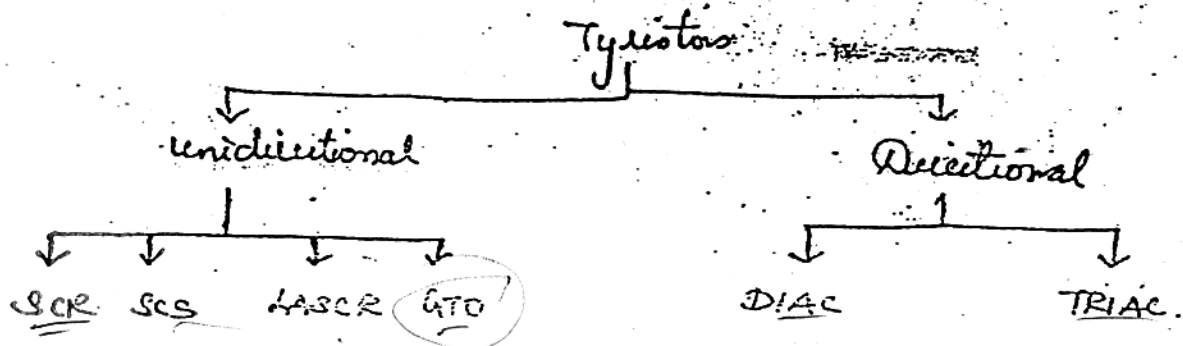
Types:-

1. Unidirectional.

Conduct in forward direction only.

2. Bidirectional

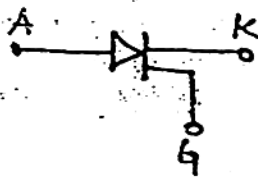
Conduct in both forward direction and reverse direction.



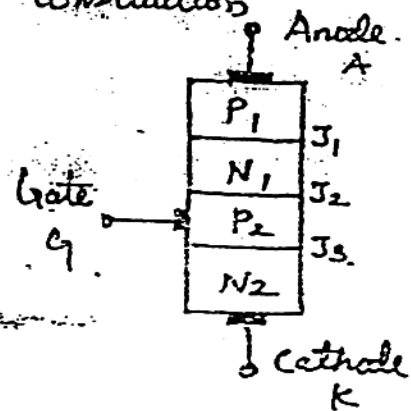
SCR (Silicon controlled rectifier)

\* Unidirectional device, allows current in only one direction

Symbol



Construction



\* The third terminal controls the operation of SCR, hence it is named as SCR (Silicon Controlled Rectifier).

Still current flows - leakage current

50 sm

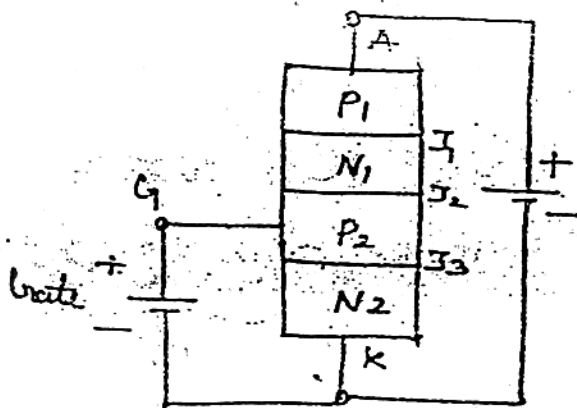
The voltage applied to Cathode w.r.t anode is called reverse voltage and SCR is in reverse blocking state.

In forward blocking state if the applied voltage is increased, the current increases till  $V_{BO}$  (Breakover voltage). Once  $V_{BO}$  is reached, the current increases as voltage decreases.

\* At this point SCR switches OFF to ON.

The minimum current required to keep the SCR in ON state holding current  $I_H$ . and corresponding voltage is  $V_H$ .

(iii) Gate is closed.



Gate is +ve w.r.t Cathode & Anode is +ve w.r.t Cathode

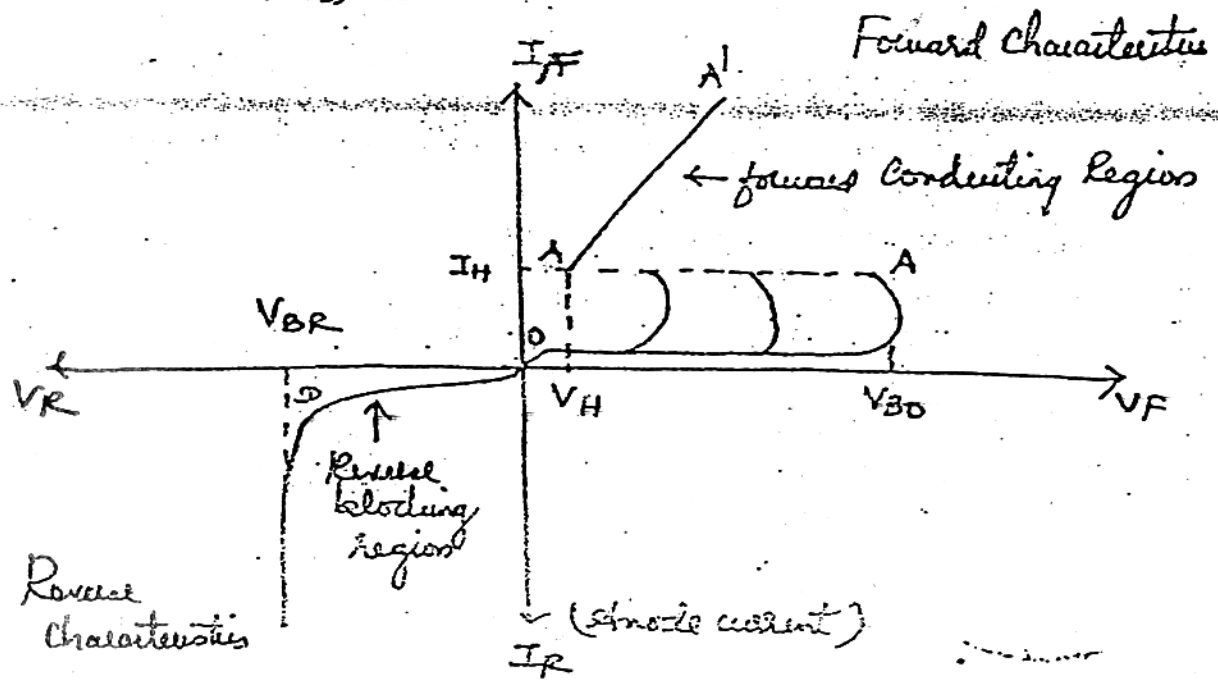
Electrons move towards +ve potential & holes move towards negative potential. At junction J<sub>2</sub> → This forms Gate current.

As gate current increases, the anode current ↑  
Some electrons cross junction J<sub>2</sub>.

If base current decrease ( $I_{B2}$ ), collector current of  $Q_2$  decreases leads to decrease in collector current of  $Q_1$ .

SCR — OFF state. (no current flows from anode to cathode).

## V-I Characteristics



## Forward Characteristics

- \* SCR is in off state until it reaches  $V_{BO}$ .
- \* After  $V_{BO}$  current increases and voltage decreases SCR ON.
- \* Current at this point is  $I_H$  holding current  
↓  
to turn device ON.
- \* If anode current falls below holding current, the SCR turns OFF.

O-A Region — forward blocking region

A-A' Region — forward conducting region

Turning OFF SCR.

52/5M

SCR conducts even when the gate signal is removed. This ability is known as latching.

1. Reversing polarity of anode to cathode Voltage
2. Anode current Interruption

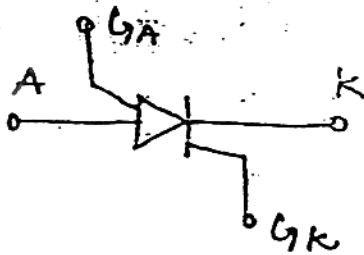
3. Reducing current of SCR below holding current.  
This method is known as forced commutation.

### Applications

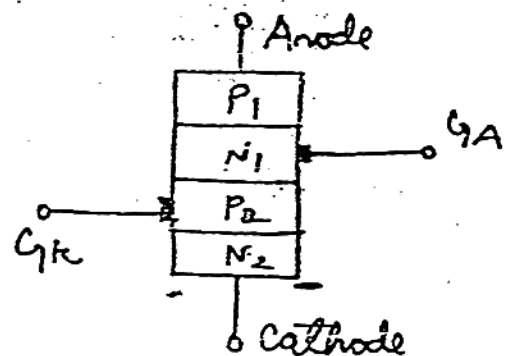
1. Motor Speed Control
2. Light dimming Control
3. Heater Control
4. Phase Control & Delay Control
5. Battery Charger.
6. Inverters & Rectifier power Supplies
7. Switches.)

### Silicon Controlled Switch (SCS)

#### Symbol



#### Construction



low power Rectifier

## Applications

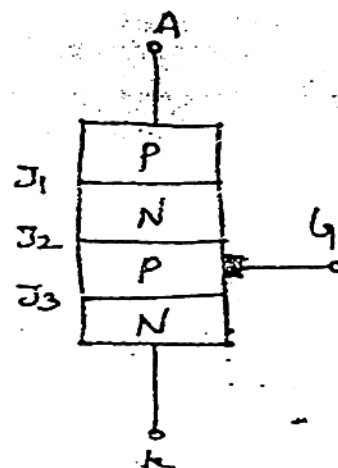
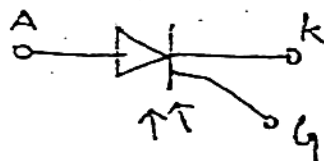
1. Counters, Registers & Timing Circuits
2. pulse generators
3. Voltage Sensors & Adapters

## LASCR

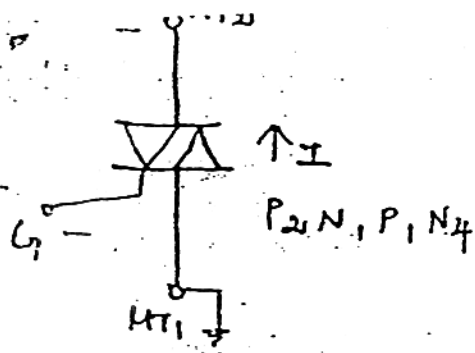
- \* Light Activated Silicon controlled Rectifier
- \* LASCR triggered or turned ON by light instead of gate current.
- \* Also called as photo thyristor.
- \* Light Activated Triac (other type of photothyristor) to ha AC currents.
- \* Sometimes both Light Source and gate signal is used to trigger SCR.
- \* If higher voltage (current) bias, the lower light intensity is required. or vice versa

## Construction

### Symbol



Construction diagrams.



4.  $M T_2$  is Negative &  $G_2$  is <sup>Negative</sup> positive SM

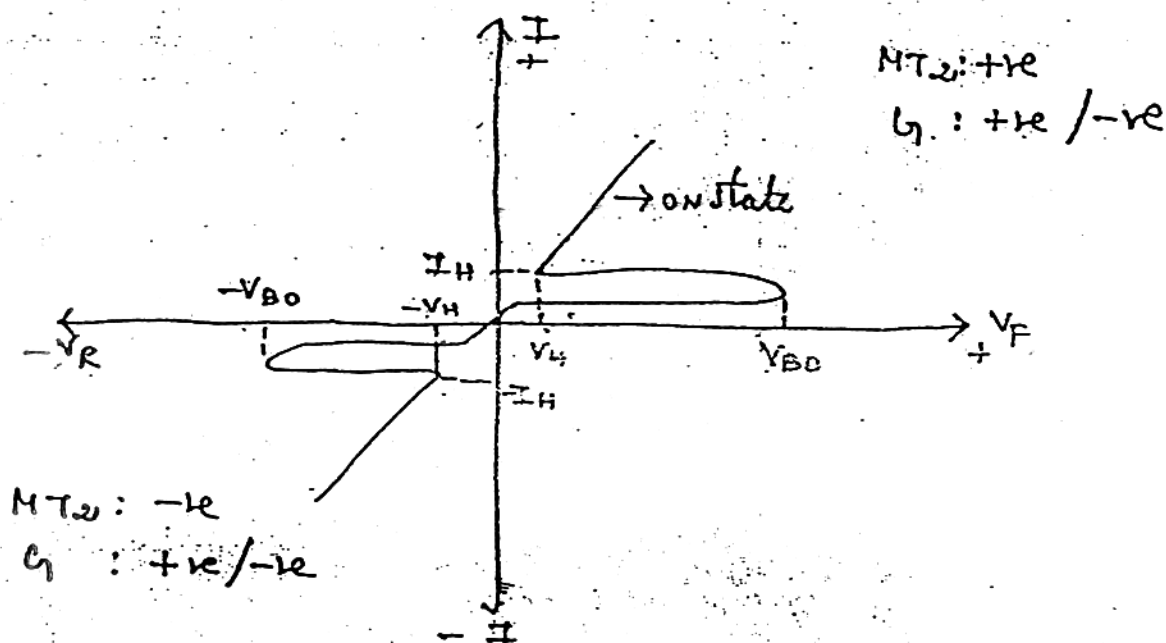
Current flows from  $M T_1$  to  $M T_2$

ie.,  $P_2 N_1 P_1 N_4$

Slightly less efficient than mode 1

Modes 1 & 4 are efficient modes in triac operation called normal modes of operation

V-I Characteristics



TRIAC is OFF until it reaches  $V_{BO}$  voltage. after that device conducts turns ON.

Both Curves are Symmetrical & identical.

Applications

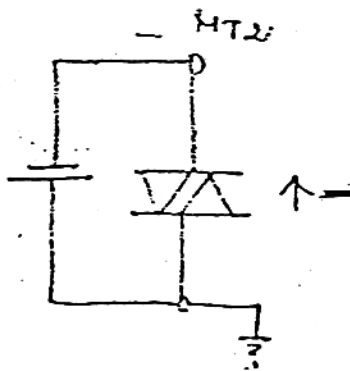
Phase Control

Motor Speed Control

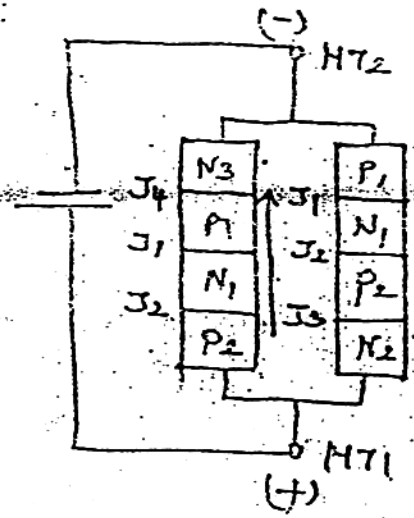
Heater Control.

Light dimming Control

Static Switch (to turn power ON and OFF.)

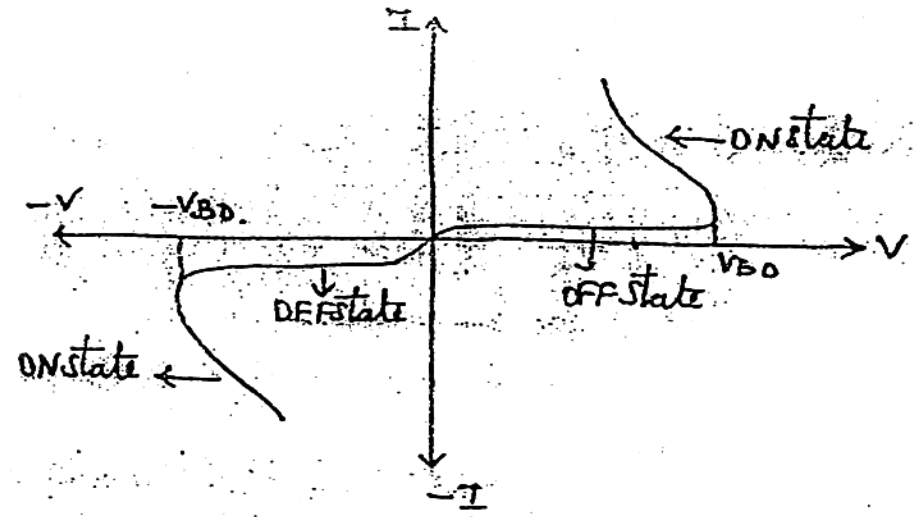


When the applied voltage is negative (H<sub>2</sub> with respect to H<sub>1</sub>), diode conducts and current passes through the diode P<sub>2</sub>N<sub>1</sub>P<sub>1</sub>N<sub>3</sub> from H<sub>1</sub> to H<sub>2</sub>.



J<sub>2</sub>, J<sub>4</sub> - forward biased  
J<sub>1</sub>, J<sub>3</sub> - reverse biased

### V-I Characteristics of DIAC



### Applications

- \* Triggering device in phase power control systems
- \* Lamp dimmer circuits
- \* Heater control circuits
- \* Speed control circuits.

Problem 1: The transistor has  $I_E = 10 \text{ mA}$  and  $\alpha = 0.98$ .

Determine the values of  $I_C$  and  $I_B$ .

Sol: The common base d.c. current gain  $\alpha = \frac{I_C}{I_E}$

$$\therefore I_C = \alpha I_E = (0.98) (10 \times 10^{-3})$$

$$I_C = 9.8 \text{ mA}$$

The emitter current  $I_E = I_B + I_C$

$$I_B = I_E - I_C = 10 \text{ mA} - 9.8 \text{ mA}$$

$$I_B = 0.2 \text{ mA}$$

Problem 2: If a transistor has a  $\alpha$  of 0.97, find the value of  $\beta$ .  
Similarly if  $\beta = 200$  find the value of  $\alpha$ .

Sol:

$$\text{If } \alpha = 0.97 \text{ then } \beta = \frac{\alpha}{1 - \alpha} = \frac{0.97}{1 - 0.97} = 32.33$$

$$\beta = 200 \text{ then } \alpha = \frac{\beta}{1 + \beta} = \frac{200}{201} = 0.995$$

Problem 3: When the emitter current of a transistor is changed by  $1 \text{ mA}$ , there is a change in collector current by  $0.99 \text{ mA}$ . Find the current gain of the transistor.

Sol: The current gain of the transistor is

$$\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{0.99 \times 10^{-3}}{1 \times 10^{-3}} = 0.99$$

Problem 4: In the fixed bias circuit a silicon transistor with  $\beta = 100$  is used  $V_{CC} = 6 \text{ V}$ ,  $R_C = 3 \text{ k}\Omega$ ,  $R_B = 530 \text{ k}\Omega$ . Draw the d.c. load line and determine the operating point. What is the stability factor?

(a) Dc load line:



$$I_B = \frac{V_T - V_{BE}}{R_B + (1+\beta)R_E} = \frac{1.818 - 0.2}{9.09 \times 10^3 + [(1+50) \times 100]} = 114 \mu A$$

$$\therefore I_C = \beta I_B = 50 \times 114 \times 10^{-6} = 5.7 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C - (1+\beta) I_B R_E$$

$$= 20 - [5.7 \times 10^{-3} \times 2 \times 10^3] - [1+50] \times 114 \mu A \times 100$$

$$V_{CE} = 8 \text{ V} \parallel$$

$$8 = \frac{1+\beta}{1+\beta \left[ \frac{R_E}{R_E + R_B} \right]} = \frac{1+50}{1+50 \left[ \frac{100}{100 + 9.09 \times 10^3} \right]} = 33. \parallel$$

Problem 6:- The p-FET shown in fig below has  $|I_{DSS}| = 12 \text{ mA}$  and  $|V_p| = 5 \text{ V}$ . Calculate the quiescent value of (i)  $I_D$  (ii)  $V_{DS}$  (iii)  $V_{GS}$

Sol:- Obtain expression for  $V_{GS}$

Apply KVL to  $I_p$  circuit we get

$$V_{GS} - I_D R_S = 0$$

$$V_{GS} = I_D R_S$$

To find  $I_D$ .

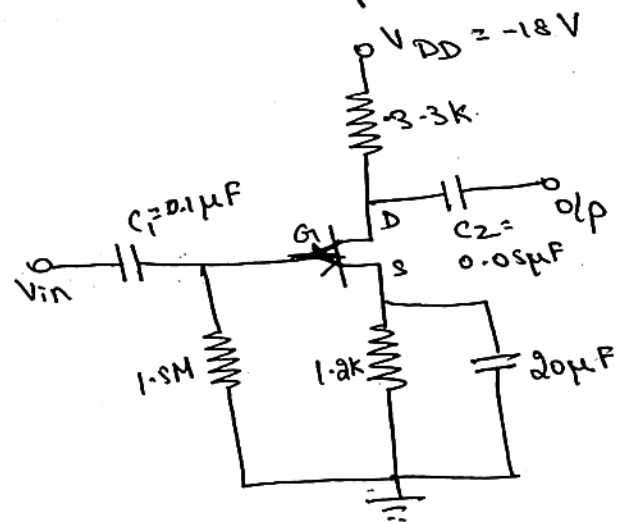
$$\text{w.k.t } I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_p} \right]^2$$

$$= 12 \text{ mA} \left[ 1 - \frac{I_D R_S}{V_p} \right]^2 = 12 \text{ mA} \left[ 1 - \frac{I_D \cdot 1.2 \text{ k}}{5} \right]^2$$

$$= 12 \text{ mA} \left[ 1 - I_D (0.24 \text{ k}) \right]^2$$

$$I_D = 12 \text{ mA} \left[ (0.24 \text{ k})^2 + (1) - 2 I_D (0.24 \text{ k}) \right]$$

solving the above expression for  $I_D$



Sol:-

$$W = 30 \mu\text{m} = 30 \times 10^{-6} \text{ m} = 30 \times 10^{-4} \text{ cm}$$

$$L = 5 \mu\text{m} = 5 \times 10^{-6} \text{ m} = 5 \times 10^{-4} \text{ cm}$$

$$K = \frac{W \mu_n C_{ox}}{2L t_{ox}} = \frac{(30 \times 10^{-4}) (650) (3.9 \times 8.85 \times 10^{-14})}{2 [5 \times 10^{-4}] [450 \times 10^{-8}]}$$

$$K = 0.1495 \text{ mA/V}^2$$

$$V_{GS} = 2V_T = 2 [0.7] = 1.4 \text{ V}$$

$$I_D = K [V_{GS} - V_T]^2 = (0.1495 \times 10^{-3}) [1.4 - 0.7]^2 = 0.0732 \text{ mA}$$

Problem 8:- The parameters of n-channel E-MOSFET are  $K = 0.2 \text{ mA/V}^2$ ,  $\lambda = 0.01 \text{ V}^{-1}$ ,  $V_T = 1.2 \text{ V}$ . Calculate the output resistance for

$$V_{GS} = 2 \text{ V}$$

$$\text{Sol:- } I_{DQ} = K [V_{GSQ} - V_T]^2 = (0.2) \times 10^{-3} [2 - 1.2]^2$$

$$I_{DQ} = 0.128 \text{ mA}$$

$$r_o = [\lambda \cdot I_{DQ}]^{-1} = [(0.01) \cdot (0.128 \times 10^{-3})]^{-1}$$

$$r_o = 781.25 \text{ k}\Omega$$

Problem 9:- Calculate the DC operating point for the circuit diagram shown below.

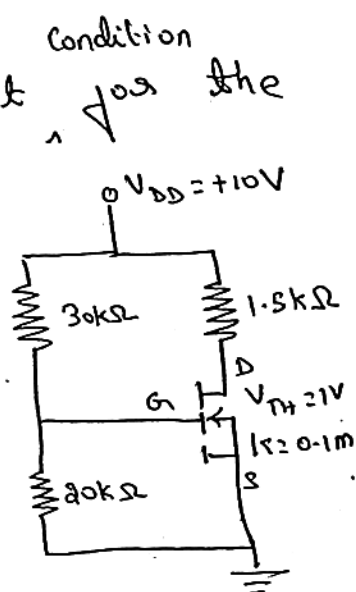
$$\text{Sol:- } \text{Given data } R_1 = 30 \text{ k}\Omega, R_2 = 20 \text{ k}\Omega$$

$$R_D = 1.5 \text{ k}\Omega \text{ \& } V_{DD} = 10 \text{ V}$$

$$V_{G1} = V_{GS} = \left[ \frac{R_2}{R_1 + R_2} \right] V_{DD}$$

$$= \left[ \frac{20 \times 10^3}{30 \times 10^3 + 20 \times 10^3} \right] 10$$

$$V_{G1} = V_{GS} = 4 \text{ V}$$



AMPLIFIERTwo port devices and the hybrid Model:-

The amplifier is a two port network having two input terminals and two output terminals, as shown below.

$I_1$  is the current to the amplifier

$V_1$  is the input voltage to amplifier

$I_2$  is the output current of the amplifier

$V_2$  is the output voltage of the amplifier.

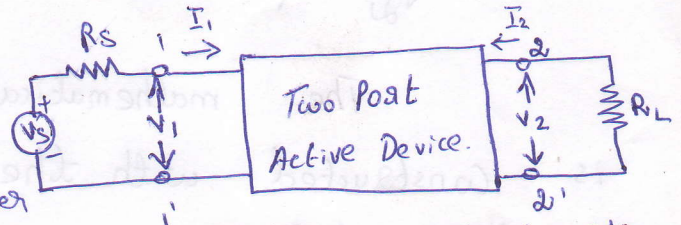


Fig. Two port network.

We know that transistor is a current control device, the input current is an independent variable. The input current,  $I_1$  and output voltage  $V_2$  defines the input voltage  $V_1$  as well as the output current  $I_2$ .

Hence input voltage  $V_1$  and output current  $I_2$  are the dependent variables, whereas input current  $I_1$  and output voltage  $V_2$  are independent variable. This can be written as

$$V_1 = f_1(I_1, V_2) \quad \text{--- (1)}$$

$$I_2 = f_2(I_1, V_2) \quad \text{--- (2)}$$

This can be written in equation form as

$$V_1 = h_{11} I_1 + h_{12} V_2 \quad \text{--- (3)}$$

$$I_2 = h_{21} I_1 + h_{22} V_2 \quad \text{--- (4)}$$

The parameters in equ (3) & (4) can be written as

$$h_{11} = \frac{V_1}{I_1} \bigg|_{V_2=0} \quad \text{--- Input resistance with output short circuited, in ohms}$$



$h_{12} = \frac{V_1}{V_2} \bigg|_{I_1=0}$  - Fraction of output voltage at input with input open circuited.

$h_{21} = \frac{I_{20}}{I_1} \bigg|_{V_2=0}$  - Forward current transfer ratio (or) current gain with output short circuited.

$h_{22} = \frac{I_{20}}{V_2} \bigg|_{I_1=0}$  - Output admittance with input open-circuited

The mathematical model for two port device is constructed with the use of four h-parameters and it is shown below.

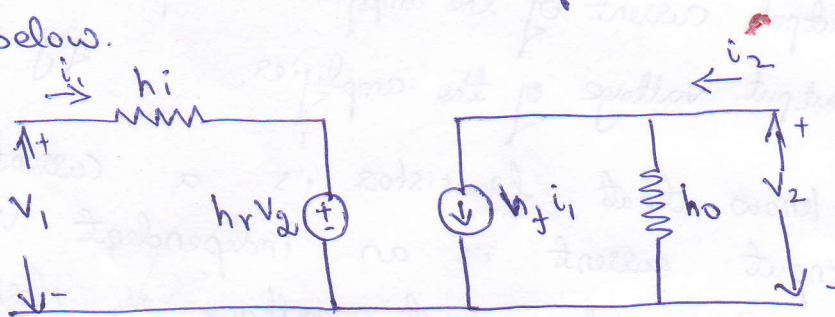


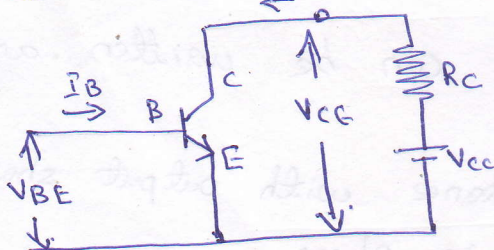
Fig. The hybrid model for two-port network

Benefits of h-parameters:

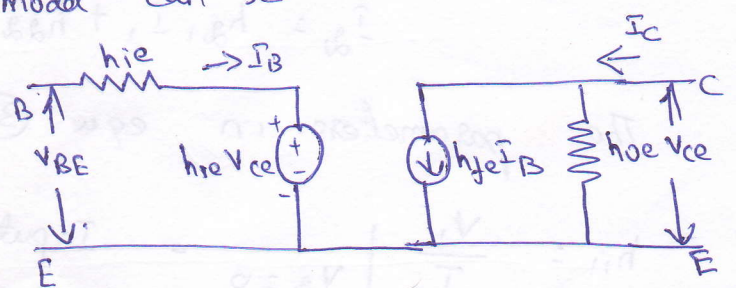
- 1) Can be obtained from the transistor static characteristic curves.
- 2) Convenient to use in circuit analysis and design.
- 3) Easy to measure.

H-Parameters model for the Common-Emitter Configuration

Consider the common emitter configuration circuit shown below. The hybrid model can be drawn as



Simple circuit for CE



H-parameter equivalent circuit.



From the h-parameter equivalent circuit of the Common emitter configuration we can write.

$$V_{BE} = h_{ie} I_B + h_{re} V_{CE} \quad \dots (5)$$

$$I_C = h_{fe} I_B + h_{oe} V_{CE} \quad \dots (6)$$

from equ (5)  $h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \bigg|_{V_{CE} = \text{constant}}$   $h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} \bigg|_{I_B = \text{constant}}$

similarly from equ (6)  $h_{fe} = \frac{\Delta I_C}{\Delta I_B} \bigg|_{V_{CE} = \text{constant}}$   $h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}} \bigg|_{I_B = \text{constant}}$

The h-parameter equivalent circuit for other two Configuration can be drawn as.

Common Collector:-

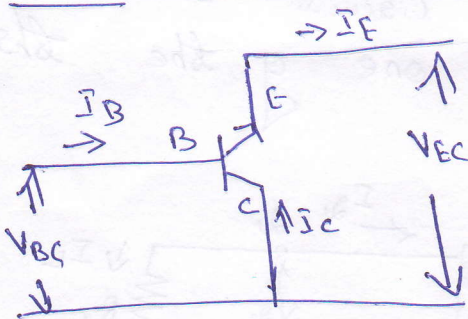


Fig. Equivalent Circuit

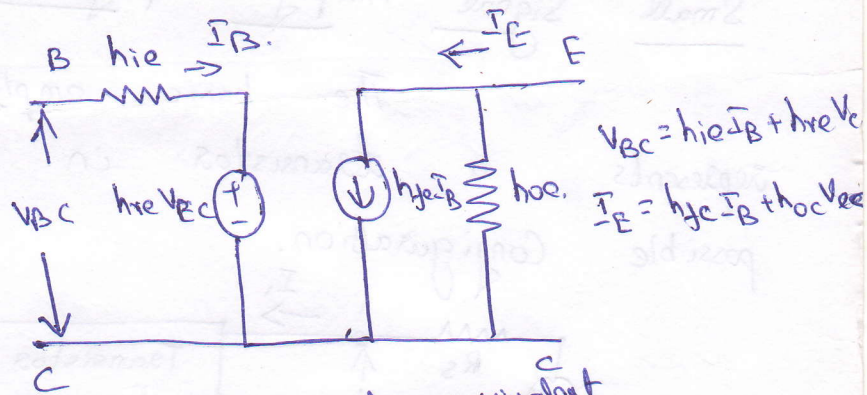
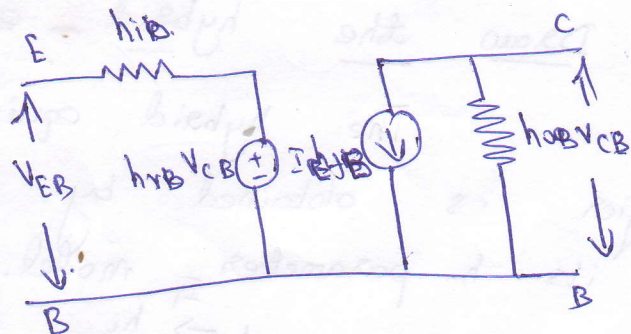
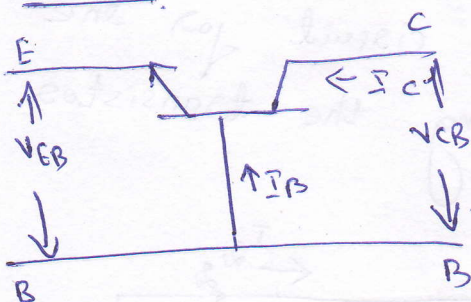


Fig. h-parameter equivalent circuit.

$$V_E = h_{ie} I_B + h_{re} V_E$$

$$I_E = h_{fe} I_B + h_{oe} V_E$$

Common Base:-



$$V_{EB} = h_{ib} I_E + h_{rb} V_C$$

$$I_C = h_{fb} I_E + h_{ob} V_C$$



# Relationship between h-parameter of different transistor Configuration. :-

## CE to CB Conversion

$$h_{ib} = \frac{h_{ie}}{1+h_{fe}}$$

$$h_{rb} = \frac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}$$

$$h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$$

$$h_{ob} = \frac{h_{oe}}{1+h_{fe}}$$

## CE to CC Conversion

$$h_{ic} = h_{ie}$$

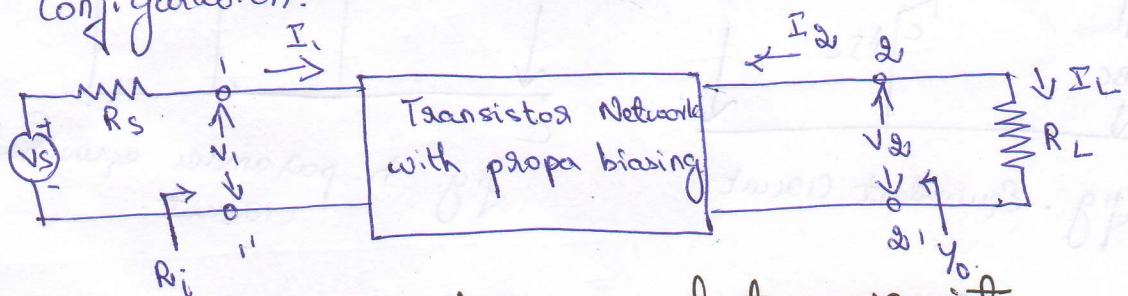
$$h_{rc} = 1 - h_{re} \approx 1$$

$$h_{fc} = -(1+h_{fe})$$

$$h_{oc} = h_{oe}$$

## Small Signal Amplifier performance in terms of h-parameters

The basic amplifier circuit shown below represents a transistor in any one of the three possible Configuration.



Step 1:-> Draw the hybrid equivalent circuit.

The hybrid equivalent circuit for the amplifier is obtained by replacing the transistor by its h-parameter model.

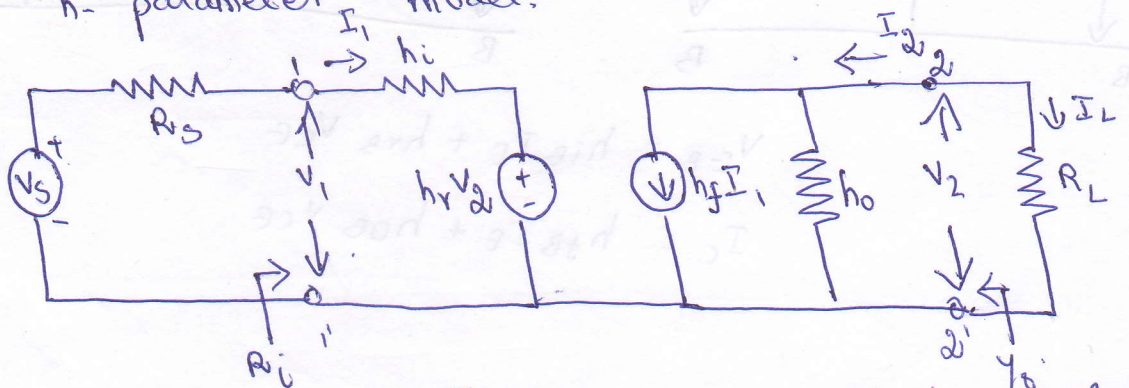


fig. Transistor amplifier in its h-parameter model

Step 2: Obtain expression for current gain ( $A_I$ ):-

In a transistor amplifier,  $A_I$  can be defined as the ratio of output to input current it is given by.

$$A_I = \frac{I_L}{I_1} \quad \text{[without considering source resistance]} \quad (1)$$

from the h-parameter model circuit we can write.

$$I_L = -I_2 \quad \text{[Both are in same magnitude but opposite direction]}$$

Substitute  $I_L$  in equ (1) we get.

$$A_I = \frac{-I_2}{I_1} \quad (2)$$

The output current  $I_2$  can be written from h-parameter model as.

$$I_2 = h_f I_1 + h_o V_2 \quad (3)$$

w.k.t  $V_2 = I_L R_L = (-I_2) R_L$

Now substitute  $V_2$  in equ (3) we get.

$$I_2 = h_f I_1 - I_2 (R_L h_o) \quad (4)$$

rearrange equ (4) and obtain " $I_2$ ".

$$I_2 + I_2 (R_L h_o) = h_f I_1$$

$$I_2 [1 + (R_L h_o)] = h_f I_1$$

$$\therefore \frac{I_2}{I_1} = \frac{h_f}{1 + h_o R_L} \quad (5)$$

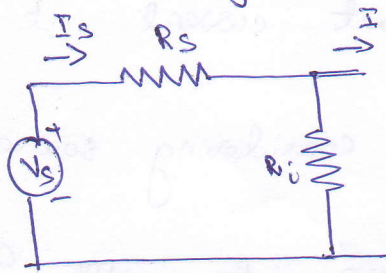
Substitute equ (5) in (2) we get.

$$A_I = \frac{-h_f}{1 + h_o R_L} \quad (6)$$

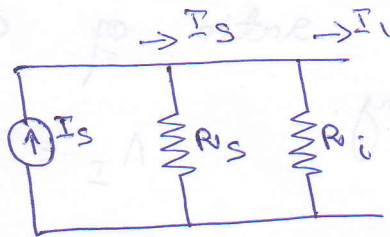


Step 3: Find Current gain including source resistance ( $A_{IS}$ )

To obtain the overall current gain change the voltage into current at input side.



(a) Input section



(b) Input section with current source instead of voltage source.

Apply current divider rule to the above circuit we get

$$I_i = \left[ \frac{R_s}{R_i + R_s} \right] I_s \quad \dots (9)$$

$$\therefore \frac{I_i}{I_s} = \frac{R_s}{R_i + R_s} \quad \dots (8)$$

For the h-parameter model the  $A_{IS}$  can be written as

$$A_{IS} = \frac{I_L}{I_s} = \frac{-I_2}{I_s} = \frac{-I_2}{I_i} \times \frac{I_i}{I_s} = A_I \times \frac{I_i}{I_s} \quad \dots (9)$$

Now substitute equ (8) in (9) we get -

$$A_{IS} = A_I \left[ \frac{R_s}{R_i + R_s} \right] \quad \dots (10)$$

Step 4: Obtain expression for input resistance ( $R_i$ ):-

Consider the input terminal of the h-parameter model.

$$R_i = \frac{V_i}{I_i} \quad \dots (11)$$

Obtain an expression for  $V_i$  in the input



circuit we get.

$$V_i = h_i I_i + h_r V_o \quad \text{--- (12)}$$

Now substitute equ (12) in (11) we get

$$R_i = \frac{h_i I_i + h_r V_o}{I_i} = h_i + h_r \frac{V_o}{I_i} \quad \text{--- (13)}$$

w.k.t

$$V_o = -I_o R_L$$

Similarly from current gain expression (2)

$$A_I = \frac{-I_o}{I_i} \Rightarrow -I_o = A_I I_i$$

Substitute  $-I_o$  in above expression we get.

$$V_o = A_I I_i R_L$$

Now substitute  $V_o$  in equ (13) we get.

$$R_i = h_i + h_r \frac{A_I I_i R_L}{I_i} = h_i + h_r A_I R_L$$

$$R_i = h_i + h_r \left[ \frac{-h_f}{1 + h_o R_L} \right] R_L$$

$$R_i = h_i - \frac{h_r h_f R_L}{1 + h_o R_L} \quad \text{--- (14)}$$

Now rearrange the above expression we get.

$$R_i = h_i - \frac{h_r h_f R_L}{R_L \left[ \frac{1}{R_L} + h_o \right]} \quad \left[ Y_L = \frac{1}{R_L} \right]$$

$$R_i = h_i - \frac{h_r h_f}{Y_L + h_o} \quad \text{--- (15)}$$

Step 5: Obtain expression for voltage gain ( $A_V$ ):-

Voltage gain is defined as the ratio of output voltage to input voltage.

$$A_V = \frac{V_o}{V_i} = \frac{V_{o2}}{V_1} \quad \text{--- (16)}$$

w.k.t  $V_{o2} = A_I I_1 R_L$

$$\therefore A_V = \frac{A_I I_1 R_L}{V_1} = \frac{A_I R_L}{V_1 / I_1} = \frac{A_I R_L}{R_i}$$

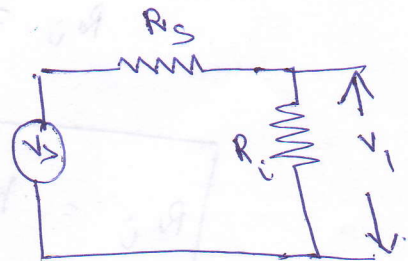
$$\therefore A_V = A_I \frac{R_L}{R_i} \quad \text{--- (17)}$$

Step 6: Obtain voltage gain including source resistance.

$$\therefore A_{VS} = \frac{V_{o2}}{V_S} = \frac{V_{o2}}{V_1} \times \frac{V_1}{V_S} = A_V \cdot \frac{V_1}{V_S} \quad \text{--- (18)}$$

Now Consider the input circuit of h-parameter model apply potential divider theorem.

$$\therefore V_1 = \left[ \frac{R_i}{R_S + R_i} \right] V_S$$



$$\therefore \frac{V_1}{V_S} = \frac{R_i}{R_S + R_i} \quad \text{--- (19)}$$

Now substitute equ (19) in (18) we get.

$$A_{VS} = A_V \left[ \frac{R_i}{R_S + R_i} \right] \quad \text{--- (20)}$$

Now substitute equ (17) in (20) we get.



$$A_{vs} = A_I \left( \frac{R_L}{R_i} \right) \left[ \frac{R_i}{R_s + R_i} \right] \quad (5)$$

$$\therefore A_{vs} = A_I \left[ \frac{R_L}{R_s + R_i} \right] \quad (21)$$

Step 1:- Obtain the expression for output admittance ( $Y_o$ )

The output admittance can be defined as the ratio of output current to output voltage

$$\therefore Y_o = \frac{I_2}{V_2} \quad \text{with } V_s = 0. \quad (22)$$

w.k.t expression for  $I_2$  can be written as

$$I_2 = h_f I_1 + h_o V_2$$

$$\therefore Y_o = \frac{h_f I_1 + h_o V_2}{V_2} = h_o + h_f \frac{I_1}{V_2} \quad (23)$$

Now apply KVL to the input loop of h-parameter model we get.

$$R_s I_1 + h_i I_1 + h_r V_2 = 0.$$

$$I_1 [R_s + h_i] + h_r V_2 = 0$$

$$I_1 [R_s + h_i] = -h_r V_2$$

$$\frac{I_1}{V_2} = \frac{-h_r}{[R_s + h_i]} \quad (24)$$

Substitute equ (24) in (23) we get.

$$Y_o = h_o - \frac{h_f h_r}{[R_s + h_i]} \quad (25)$$

Step 8:- Obtain expression for power gain ( $A_p$ ):-

Power gain is defined as the ratio of average power delivered to the load  $R_L$  to the input power.

$$A_p = \frac{P_2}{P_1} = \frac{-V_2 I_2}{V_1 I_1} = A_V A_I \quad \text{--- (26)}$$

Substitute eqn (17) in (26) we get.

$$A_p = A_I A_I \frac{R_L}{R_i} = A_I^2 \frac{R_L}{R_i} \quad \text{--- (27)}$$

Step 9:- Relation between  $A_{VS}$  and  $A_{IS}$

Consider equation (10) and (21)

$$\frac{A_{VS}}{A_{IS}} = \frac{A_I \left[ \frac{R_L}{R_i + R_s} \right]}{A_I \left[ \frac{R_s}{R_i + R_s} \right]} = \frac{R_L}{R_s}$$

$$\therefore A_{VS} = A_{IS} \left[ \frac{R_L}{R_s} \right] \quad \text{--- (28)}$$

Resultant Expressions:-

$$A_I = \frac{-h_f}{1 + h_o R_L}$$

$$A_{IS} = A_I \left[ \frac{R_s}{R_i + R_s} \right]$$

$$R_i = h_i - \frac{h_r h_f}{h_o + Y_L}$$

$$A_V = A_I \frac{R_L}{R_i}$$

$$A_{VS} = A_V \left[ \frac{R_i}{R_i + R_s} \right] = A_I \left[ \frac{R_L}{R_i + R_s} \right]$$

$$Y_o = h_o - \frac{h_r h_f}{h_i + R_s}$$

$$R_o = \frac{1}{Y_o}$$

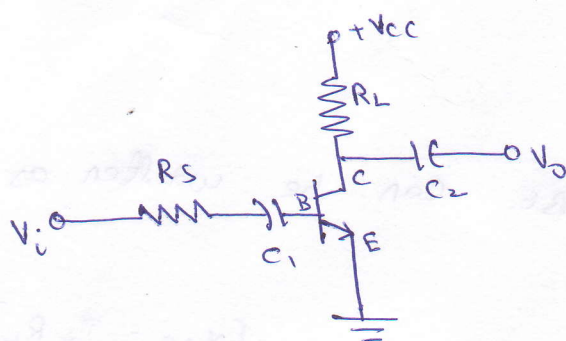
$$A_p = A_I^2 \frac{R_L}{R_i}$$

$$A_{VS} = A_{IS} \left[ \frac{R_L}{R_s} \right]$$

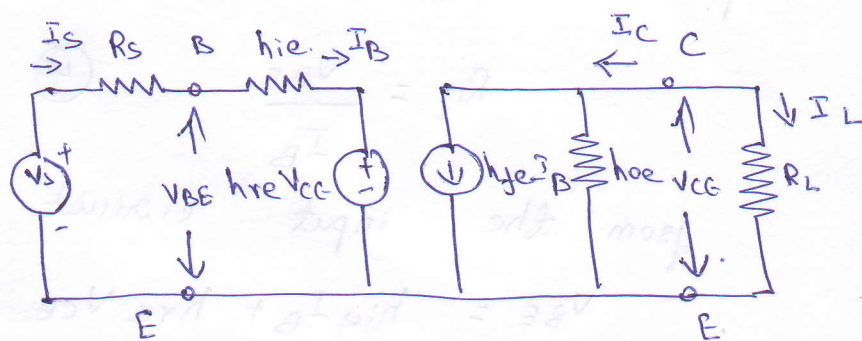


# h-parameter model for CE amplifier:-

The circuit diagram of a CE amplifier and its equivalent h-parameter model is shown below.



(a) CE amplifier.



(b) h-parameter model.

Step 1:- obtain expression for  $A_I$ :-

$$\text{Current gain } A_I = \frac{I_L}{I_B} = \frac{-I_C}{I_B} \quad \dots (1)$$

w.k.t output current can be written as

$$I_C = h_{fe} I_B + h_{oe} V_{CE} \quad \dots (2)$$

$$\text{w.k.t } V_{CE} = I_L R_L$$

$$\therefore I_C = h_{fe} I_B + h_{oe} I_L R_L$$

$$= h_{fe} I_B + h_{oe} I_C R_L$$

$$I_C + h_{oe} I_C R_L = h_{fe} I_B$$

$$I_C [1 + h_{oe} R_L] = h_{fe} I_B$$

$$\therefore \frac{I_C}{I_B} = \frac{h_{fe}}{1 + h_{oe} R_L} \quad \dots (3)$$

Now substitute equ (3) in (1) we get.

$$A_I = \frac{-h_{fe}}{1 + h_{oe} R_L} \quad \dots (4)$$

Step 2:- Obtain expression for input resistance ( $R_i$ )

From the h-parameter equivalent circuit the input resistance can be written as

$$R_i = \frac{V_{BE}}{I_B} \quad \text{--- (4)}$$

from the input circuit  $V_{BE}$  can be written as

$$V_{BE} = h_{ie} I_B + h_{re} V_{CE}$$

$$= h_{ie} I_B + h_{re} [I_L R_L]$$

$$[V_{CE} = I_L R_L]$$

$$= h_{ie} I_B - h_{re} I_C R_L$$

$$[-I_C = I_L]$$

$$V_{BE} = h_{ie} I_B + h_{re} A_I I_B R_L \quad \text{--- (5)}$$

$$A_I = -\frac{I_C}{I_B}$$

Substitute equ (5) in (4) we get.

$$R_i = \frac{[h_{ie} I_B + h_{re} A_I I_B R_L]}{I_B}$$

$$\therefore R_i = h_{ie} + h_{re} A_I R_L \quad \text{--- (6)}$$

Now substitute equ (4) in (6) we get.

$$R_i = h_{ie} - \frac{h_{re} h_{fe} R_L}{1 + h_{oe} R_L} \quad \text{--- (7)}$$

Step 3:- Obtain an expression for voltage gain ( $A_V$ )

From the h-parameter equivalent circuit

Voltage gain can be written as



$$A_V = \frac{V_{CE}}{V_{BE}} \quad \dots (8)$$

w.k.t  $V_{CE} = I_L R_L = -I_E R_L = A_I I_B R_L \quad \dots (9)$

Substitute equ (9) in (8) we get

$$A_V = \frac{A_I I_B R_L}{V_{BE}} = \frac{A_I R_L}{V_{BE}/I_B} = \frac{A_I R_L}{R_i}$$

$$\therefore A_V = A_I \frac{R_L}{R_i} \quad \dots (10)$$

Step 4 :- Obtain expression for output admittance ( $Y_o$ )

Using h-parameter model the output impedance can be written as

$$Y_o = \frac{I_c}{V_{CE}} \quad \dots (11)$$

w.k.t  $I_c = h_{fe} I_B + h_{oe} V_{CE}$

$$\therefore Y_o = \frac{h_{fe} I_B + h_{oe} V_{CE}}{V_{CE}} = h_{oe} + h_{fe} \frac{I_B}{V_{CE}} \quad \dots (12)$$

Assign  $V_s = 0$  and apply KVL to input circuit

$$R_s I_B + h_{ie} I_B + h_{re} V_{CE} = 0.$$

$$I_B [R_s + h_{ie}] + h_{re} V_{CE} = 0$$

$$-I_B [R_s + h_{ie}] = -h_{re} V_{CE}$$

$$\therefore \frac{I_B}{V_{CE}} = \frac{-h_{re}}{R_s + h_{ie}} \quad \dots (13)$$

Now substitute equation (13) in (12) we get.

$$Y_o = h_{oe} - \frac{h_{re} h_{fe}}{R_s + h_{ie}} \quad \dots (14)$$



$$A_V = \frac{V_{CE}}{V_{BE}} \quad \dots (8)$$

w.k.t  $V_{CE} = I_L R_L = -I_E R_L = A_I I_B R_L \quad \dots (9)$

Substitute equ (9) in (8) we get

$$A_V = \frac{A_I I_B R_L}{V_{BE}} = \frac{A_I R_L}{V_{BE}/I_B} = \frac{A_I R_L}{R_i}$$

$$\therefore A_V = A_I \frac{R_L}{R_i} \quad \dots (10)$$

Step 4 :- Obtain expression for output admittance ( $Y_o$ )

Using h-parameter model the output impedance can be written as

$$Y_o = \frac{I_c}{V_{CE}} \quad \dots (11)$$

w.k.t  $I_c = h_{fe} I_B + h_{oe} V_{CE}$

$$\therefore Y_o = \frac{h_{fe} I_B + h_{oe} V_{CE}}{V_{CE}} = h_{oe} + h_{fe} \frac{I_B}{V_{CE}} \quad \dots (12)$$

Assign  $V_s = 0$  and apply KVL to input circuit

$$R_s I_B + h_{ie} I_B + h_{re} V_{CE} = 0$$

$$I_B [R_s + h_{ie}] + h_{re} V_{CE} = 0$$

$$I_B [R_s + h_{ie}] = -h_{re} V_{CE}$$

$$\therefore \frac{I_B}{V_{CE}} = \frac{-h_{re}}{R_s + h_{ie}} \quad \dots (13)$$

Now substitute equation (13) in (12) we get

$$Y_o = h_{oe} - \frac{h_{re} h_{fe}}{R_s + h_{ie}} \quad \dots (14)$$



| Parameters                     | Common Emitter                                            | Common Collector                                          | Common Base                                               |
|--------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|
| Circuit diagram                |                                                           |                                                           |                                                           |
| h-parameter equivalent circuit |                                                           |                                                           |                                                           |
| Current gain.                  | $A_I = \frac{-h_{fe}}{1 + h_{oe} R_L}$                    | $A_I = \frac{-h_{fc}}{1 + h_{oc} R_L}$                    | $A_I = \frac{-h_{fb}}{1 + h_{ob} R_L}$                    |
| Input resistance               | $R_i = h_{ie} - \frac{h_{fe} h_{re} R_L}{1 + h_{oe} R_L}$ | $R_i = h_{ic} - \frac{h_{fc} h_{rc} R_L}{1 + h_{oc} R_L}$ | $R_i = h_{ib} - \frac{h_{fb} h_{rb} R_L}{1 + h_{ob} R_L}$ |
| Voltage gain.                  | $A_V = A_I \frac{R_L}{R_i}$                               | $A_V = A_I \frac{R_L}{R_i}$                               | $A_V = A_I \frac{R_L}{R_i}$                               |
| Output admittance              | $Y_o = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_S}$       | $Y_o = h_{oc} - \frac{h_{fc} h_{rc}}{h_{ic} + R_S}$       | $Y_o = h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib} + R_S}$       |



Problem 1:- Consider a single stage CE amplifier with  $R_S = 1k$  and  $R_L = 1.2k\Omega$ . Calculate  $A_I$ ,  $R_i$ ,  $A_v$ ,  $A_{IS}$ , power gain and  $R_o$  if  $h_{ie} = 1.1k$ ,  $h_{re} = 2.5 \times 10^{-4}$ ,  $h_{fe} = 50$  and  $h_{oe} = 25 \mu A/V$ .

Solution:-

$$A_I = \frac{-h_{fe}}{1 + h_{oe}R_L} = \frac{-50}{1 + (25 \times 10^{-6} \times 1.2 \times 10^3)} = -48.54$$

$$R_i = h_{ie} + h_{re}A_I R_L = 1.1 \times 10^3 + [2.5 \times 10^{-4} \times -48.54 \times 1.2 \times 10^3] = 1.08k\Omega$$

$$A_v = A_I \frac{R_L}{R_i} = -48.54 \times \left[ \frac{1.2 \times 10^3}{1.08 \times 10^3} \right] = -53.663$$

$$A_{vs} = A_v \left[ \frac{R_i}{R_S + R_i} \right] = -53.66 \times \left[ \frac{1.08 \times 10^3}{1 \times 10^3 + 1.08 \times 10^3} \right] = -27.93$$

$$A_{IS} = A_I \left[ \frac{R_S}{R_S + R_i} \right] = -48.54 \times \left[ \frac{1 \times 10^3}{1 \times 10^3 + 1.08 \times 10^3} \right] = -23.28$$

$$Y_o = h_{oe} - \frac{h_{fe}h_{re}}{h_{ie} + R_S} = 25 \times 10^{-6} - \frac{[50 \times 2.5 \times 10^{-4}]}{[1.1 \times 10^3 + 1 \times 10^3]} = 19.0 \mu A/V$$

$$R_o = \frac{1}{Y_o} = \frac{1}{19 \times 10^{-6}} = 52.6k\Omega$$

$$A_p = A_I^2 \left[ \frac{R_L}{R_i} \right] = (-48.54)^2 \times \left[ \frac{1.2 \times 10^3}{1.08 \times 10^3} \right] = 2.62 \times 10^3$$

Problem 2:- In a common collector circuit shown below has a transistor parameters are  $h_{ic} = 1.2k$ ,  $h_{fc} = -101$ ,  $h_{rc} = 1$  and  $h_{oc} = 25 \mu A/V$ . Calculate the  $R_i$ ,  $A_I$ ,  $A_v$ ,  $A_{vs}$  and  $R_o$  for the circuit.

Solution:

(i) Current gain ( $A_I$ ) =  $\frac{-I_E}{I_B} = \frac{-h_{fc}}{1+h_{oc}R_L'}$

$$R_L' = R_E \parallel R_L$$

$$A_I = \frac{-(-101)}{1 + \left[ 25 \times 10^{-6} (5 \times 10^3 \parallel 20 \times 10^3) \right]}$$

$$A_I = 91.81$$

(ii) Input resistance  $R_i = h_{ie} + h_{re} A_I R_L'$

$$= 1.2 \times 10^3 + \left[ 1 \times 91.81 \times (5 \times 10^3 \parallel 20 \times 10^3) \right] = 368.44 \text{ k}$$

(iii) Overall input resistance

$$R_{i1} = R_i \parallel R_1 \parallel R_2 = (368.44 \text{ k} \parallel 10 \times 10^3 \parallel 10 \times 10^3) = 4.93 \text{ k}$$

(iv) Voltage gain.

$$A_V = \frac{A_I R_L'}{R_i} = 91.81 \cdot \left[ \frac{(30 \times 10^3 \parallel 20 \times 10^3)}{368.44 \times 10^3} \right] = 0.996 \parallel$$

(v) Overall voltage gain

$$A_{Vs} = \frac{V_o}{V_s} = \frac{V_o}{V_{BE}} \times \frac{V_{BE}}{V_s} = A_V \cdot \frac{V_{BE}}{V_s}$$

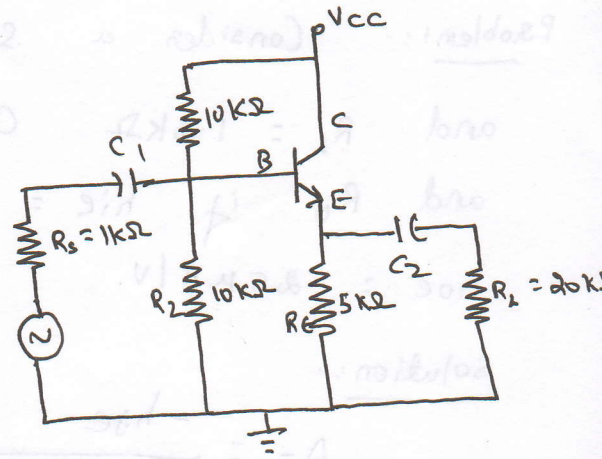
$$= A_V \cdot \frac{R_{i1}}{R_{i1} + R_s} = 0.996 \left[ \frac{4.93 \times 10^3}{(4.93 \times 10^3 + 1 \times 10^3)} \right] = 0.828$$

(vi) Overall current gain:

$$A_{Is} = \frac{I_L}{I_s} = \frac{I_L}{I_E} \times \frac{I_E}{I_B} \times \frac{I_B}{I_s}$$

$$\frac{I_L}{I_E} = \frac{-R_E}{R_E + R_L} = \frac{-5 \times 10^3}{5 \times 10^3 + 20 \times 10^3} = -0.2$$

$$\frac{I_E}{I_B} = -A_I = -91.81$$





$$\frac{I_B}{I_S} = \frac{R_S}{R_B + R_S} = \frac{(1 \times 10^3)}{[10k \parallel 10k] + (1 \times 10^3)} = 0.167$$

$$A_{IS} = (-91.81) \times \left( \frac{-0.2}{1} \right) \times (0.167) = 3.07$$

g) Output resistance

$$R_o = \frac{1}{h_{oe} - \left( \frac{h_{fe} h_{re}}{h_{ie} + R_S'} \right)}$$

$$\begin{aligned} R_S' &= R_S \parallel R_1 \parallel R_2 \\ &= 1k \parallel 10k \parallel 10k \\ &= 833.33 \Omega \end{aligned}$$

$$= \frac{1}{25 \times 10^{-6} - \left[ \frac{-101 \times 1}{1.2 \times 10^3 + 833.33} \right]} = 20.12 \Omega$$

$$R_o' = R_o \parallel R_L'$$

$$= 20.12 \parallel [5 \times 10^3 \parallel 20 \times 10^3] = 20 \Omega$$

Analysis of Transistor amplifier Configuration using Simplified h-parameter model.

In h-parameter model the admittance  $h_o$  is in parallel with  $R_L$ . The parallel combination of two unequal impedance ie  $h_o$  and  $R_L$  is approximately equal to lower value. That is  $h_o \gg R_L$  then the term  $h_o$  can be neglected.

If  $h_o$  is neglected then the output current can be written as

$$I_o = h_f I_i$$

Similarly the magnitude of voltage is.

$$h_r V_o = -h_r I_o R_L = -h_r h_f I_i R_L$$

where  $h_{re} h_i \approx 0.01$  so it can be neglected in comparison with voltage drop across  $h_i$

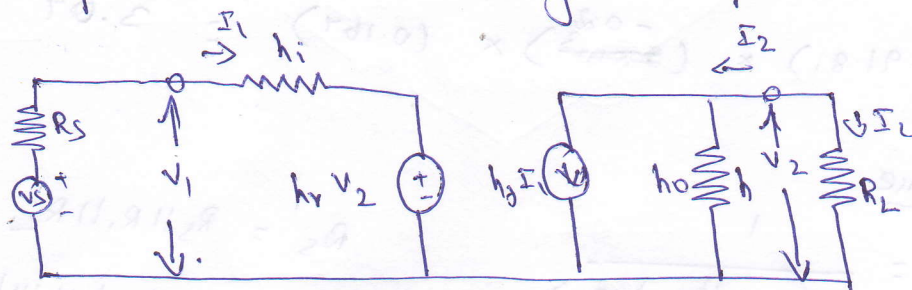


Fig. h-parameter model for two port network.

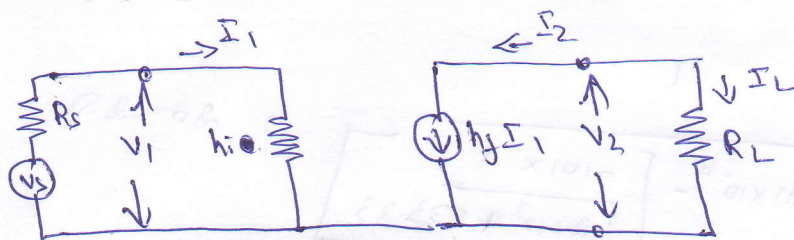
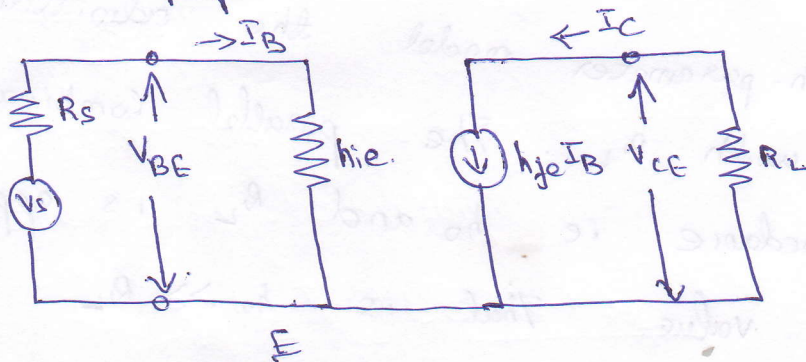


Fig. Approximate h-parameter model.

Analysis of CE amplifier using approximate model:-

The circuit diagram for approximate model for CE amplifier is shown below.



We know that for a CE amplifier the current gain can be written as

$$A_I = \frac{-h_{fe}}{1 + h_{oe} R_L} \quad \text{--- (1)}$$

In approximate model  $h_{oe}$  is neglected therefore current gain become.



$$A_I = -h_{fe} \quad \dots (2)$$

Input Impedance:-

The input impedance for the CE amplifier can be written as

$$R_i = h_{ie} - \frac{h_{re} h_{fe}}{h_{oe} + Y_L} \quad \dots (3)$$

In approximate h-parameter model we neglect  $h_{re}$  and  $h_{oe}$  we get.

$$R_i = h_{ie} \quad \dots (4)$$

Voltage Gain:-

The voltage gain for the approximate h-parameter model can be written as

$$A_V = A_I \left( \frac{R_L}{R_i} \right) \quad \dots (5)$$

Output Impedance:-

The output impedance for the CE amplifier can be written as

$$Y_o = h_{oe} - \frac{h_{re} h_{fe}}{h_{ie} + R_s} \quad \dots (6)$$

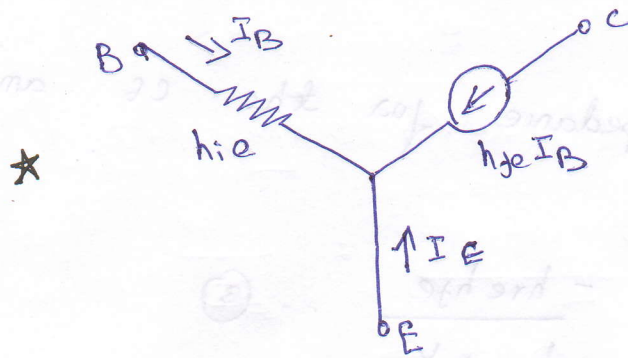
In approximate h-parameter model we neglect  $h_{re}$  and  $h_{oe}$  therefore.

$$Y_o = 0 \quad \dots (7)$$

Output Resistance:-

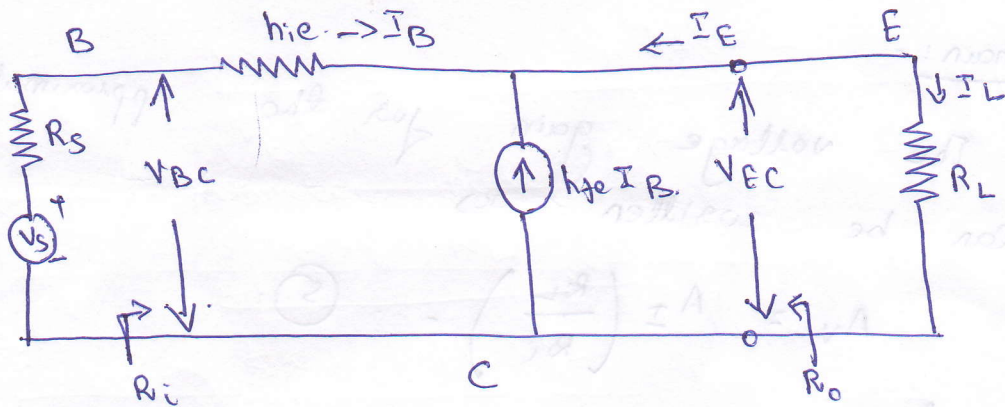
$$R_o = \frac{1}{Y_o} = \frac{1}{0} = \infty \quad \dots (8)$$

Approximate hybrid model for all the configuration



Analysis of CC amplifier using approximate model:-

The circuit diagram for CC amplifier using approximate h-parameter model is shown below.



i) Current gain:-

From the above circuit diagram, the current through the load resistance.

$$I_L = h_{fe} I_B + I_B = I_B [1 + h_{fe}] \quad \dots (1)$$

∴ The current gain can be obtained by.

$$A_I = \frac{I_L}{I_B} = \frac{I_B [1 + h_{fe}]}{\cancel{I_B}} = 1 + h_{fe} \quad \dots (2)$$

ii) Input resistance:-

From the above circuit diagram the voltage  $V_{BC}$  can be written as



$$V_{BC} = h_{ie} I_B + [1 + h_{fe}] I_B R_L \quad \dots (3)$$

The input resistance can be written as

$$R_i = \frac{V_{BC}}{I_B} = \frac{h_{ie} I_B + (1 + h_{fe}) I_B R_L}{I_B}$$

$$R_i = h_{ie} + (1 + h_{fe}) R_L \quad \dots (4)$$

Voltage gain:

Voltage gain for the CC amplifier can be written as

$$A_V = \frac{V_{EC}}{V_{BC}} = \frac{(1 + h_{fe}) I_B R_L}{h_{ie} I_B + [1 + h_{fe}] I_B R_L}$$

$$A_V = \frac{(1 + h_{fe}) R_L}{h_{ie} + (1 + h_{fe}) R_L} \quad \dots (5)$$

in the above expression.  $(1 + h_{fe}) R_L \gg h_{ie}$ .

$$\therefore A_V = \frac{(1 + h_{fe}) R_L}{(1 + h_{fe}) R_L} = 1 \quad \dots (6)$$

output Resistance:  $(R_o)$

It is the ratio of output voltage to output current with  $V_s = 0$ .

$$\therefore R_o = \frac{V_{EE}}{I_E} \Big|_{V_s = 0} \quad \dots (7)$$

Now apply KVL to the CC approximate model circuit diagram. we get.



$$I_B R_S + I_B h_{ie} + V_{CE} = V_S \quad V_S = 0$$

$$\therefore I_B R_S + I_B h_{ie} + V_{CE} = 0$$

$$- I_B [R_S + h_{ie}] = + V_{CE} \quad \text{--- (8)}$$

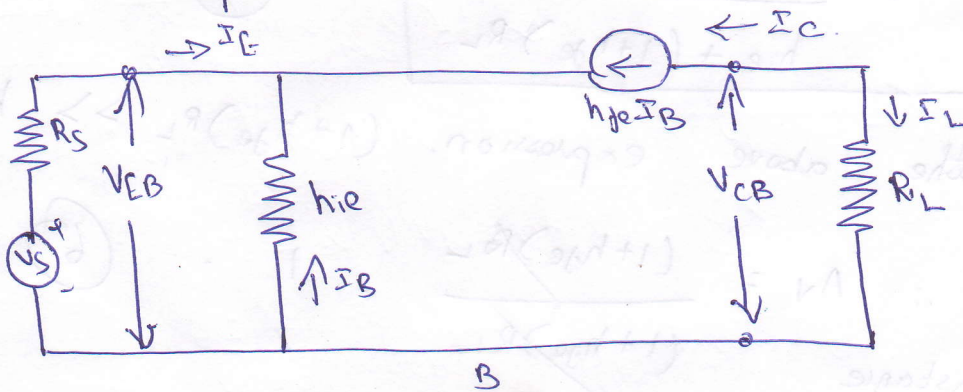
$$\text{and w.k.t } I_E = - [1 + h_{fe}] I_B \quad \text{--- (9)}$$

Now substitute equ (8) & (9) in (7) we get.

$$R_o = \frac{- I_B [R_S + h_{ie}]}{- I_B [1 + h_{fe}]} = \frac{(R_S + h_{ie})}{(1 + h_{fe})} \quad \text{--- (10)}$$

Analysis of CB amplifier using approximate h-parameter model :-

The circuit diagram for CB amplifier using approximate h-parameter model is shown below.



(i) Current gain:-

The current gain is obtained from the above circuit diagram as

$$A_I = \frac{- I_C}{I_E} = \frac{- h_{fe} I_B}{I_E} \quad \text{--- (1)}$$

from the circuit diagram.

$$I_E = - h_{fo} I_B - I_B = - [1 + h_{fe}] I_B \quad \text{--- (2)}$$

Substitute equ (2) in (1) we get.

$$A_I = \frac{-h_{fe} \cancel{I_B}}{[1+h_{fe}] \cancel{I_B}} = \frac{h_{fe}}{1+h_{fe}} \dots (3)$$

ii) Input resistance :-

The input resistance for the CB amplifier can be written as

$$R_i = \frac{V_{EB}}{I_E} = \frac{\cancel{h_{ie} I_B}}{(1+h_{fe}) \cancel{I_B}} = \frac{h_{ie}}{1+h_{fe}} \dots (4)$$

iii) Voltage gain :-

The voltage gain for the CB amplifier can be written as

$$A_V = \frac{V_{CB}}{V_{EB}} = \frac{\cancel{h_{fe} I_B R_L}}{\cancel{h_{ie} I_B}} = \left( \frac{h_{fe}}{h_{ie}} \right) R_L \dots (5)$$

iv) Output Resistance (R<sub>o</sub>) :-

The output resistance can be written as

$$R_o = \frac{V_{CB}}{I_C} \Big|_{V_S = 0} \dots (6)$$

when  $V_S = 0$ , then  $I_E$  and  $I_B = 0$  therefore  $I_C = 0$

Now substitute  $I_C = 0$  in equ (6) we get.

$$R_o = \frac{V_{CB}}{0} = \infty \dots (7)$$

Problem 3 :- A Common base amplifier, has the following components  $R_S = 600\Omega$ ,  $R_C = 5.6K$ ,  $R_E = 5.6K$ ,  $R_L = 39K$ . The transistor parameters are  $h_{ie} = 1K$ ,  $h_{fe} = 85$  and  $h_{oe} = 2\mu A/V$ . Calculate  $A_I$ ,  $R_i$ ,  $A_V$  and  $R_o$ .



Solution:

$$\text{Since } h_{oe} \times (R_C \parallel R_L) = 2 \times 10^{-6} (5.6 \times 10^3 \parallel 39 \text{ k}\Omega) \\ = 9.79 \times 10^{-3}$$

which is less than 0.1 so we can use approximate model.

$$(i) \text{ current gain } (A_I) = \frac{h_{fe}}{1+h_{fe}} = \frac{85}{1+85} = 0.988$$

$$(ii) \text{ Input resistance } R_i = \frac{h_{ie}}{1+h_{fe}} = \frac{1000}{1+85} = 11.627 \Omega$$

$$R_i' = R_E \parallel R_i = 5.6 \times 10^3 \parallel 11.63 = 11.6 \Omega$$

$$(iii) \text{ Voltage gain } (A_V) = \frac{h_{fe} R_i'}{h_{ie}} = \frac{85 [5.6 \times 10^3 \parallel 39 \times 10^3]}{1 \times 10^3}$$

$$A_V = 416.23$$

(iv) Output resistance ( $R_o$ ):

$$\text{w.k.t } R_o = \infty.$$

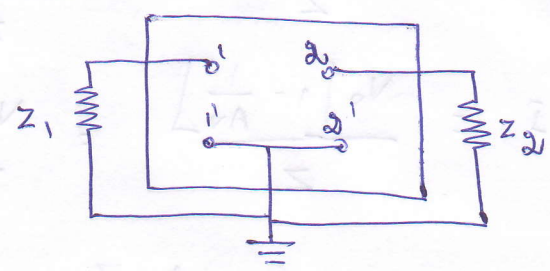
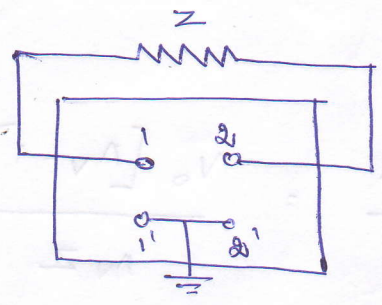
$$\text{where } R_o' = R_o \parallel R_L' = \infty \parallel (R_C \parallel R_L) \\ = \infty \parallel (5.6 \text{ k} \parallel 39 \text{ k}) \\ = 4.89 \text{ k}.$$

Millers Theorem:

Statement: Millers theorem states that when 'z' impedance connected between two nodes, can be replaced by two separate impedances  $z_1$  and  $z_2$ , where  $z_1$  is connected between node 1 and ground and  $z_2$  is connected between node 2 and ground.

where  $Z_1 = \frac{Z}{1-K}$  ;  $Z_2 = \frac{ZK}{K-1}$

"K" is voltage gain.

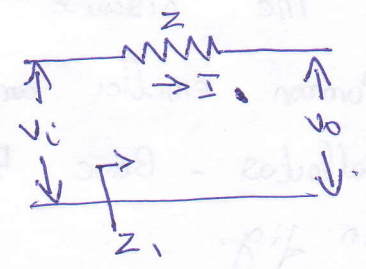


Proof for millers theorem:

According to millers theorem, the effect of impedance on input circuit is a ratio of input voltage  $V_i$  to the current  $I$  which flow from input to output

$$Z_1 = \frac{V_i}{I} \quad \text{--- (1)}$$

From the circuit diagram the current  $I$  can be written as



$$I = \frac{V_i - V_o}{Z} = \frac{V_i \left[ 1 - \frac{V_o}{V_i} \right]}{Z} = \frac{V_i [1 - A_v]}{Z}$$

$$\therefore Z_1 = \frac{V_i}{I} = \frac{Z}{1 - A_v} = \frac{Z}{1 - K}$$

$Z_1 = \frac{Z}{1-K}$

--- (2)

Similarly the effect of impedance  $Z$  on the output circuit is the ratio of output voltage to the current  $I$  is



$$Z_2 = \frac{V_o}{I}$$

from the circuit diagram

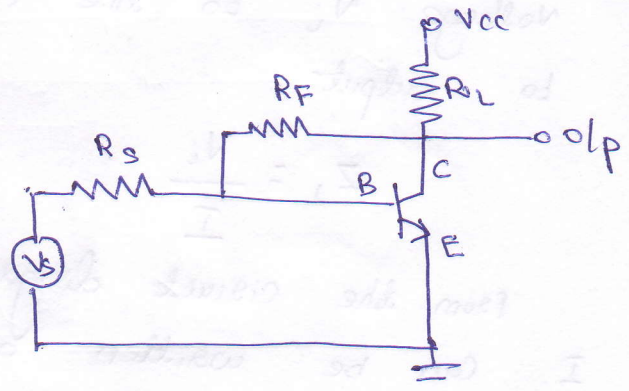
$$I = \frac{V_o - V_i}{Z} = \frac{V_o \left[ 1 - \frac{V_i}{V_o} \right]}{Z}$$

$$I = \frac{V_o \left[ 1 - \frac{1}{A_v} \right]}{Z} = \frac{V_o \left[ \frac{A_v - 1}{A_v} \right]}{Z} = \frac{V_o [A_v - 1]}{A_v Z}$$

$$\therefore Z_2 = \frac{V_o}{I_1} = \frac{A_v Z}{A_v - 1} = \frac{k Z}{(k - 1)} //$$

### Analysis of CE amplifier with Collector to Base Bias

The circuit diagram for common emitter amplifier with collector - base bias is shown in fig.



In collector to base bias circuit the resistance  $R_F$  is connected between input and output.

fig. Collector - Base Bias

Draw the h-parameter equivalent circuit for collector to base bias using approximate model.

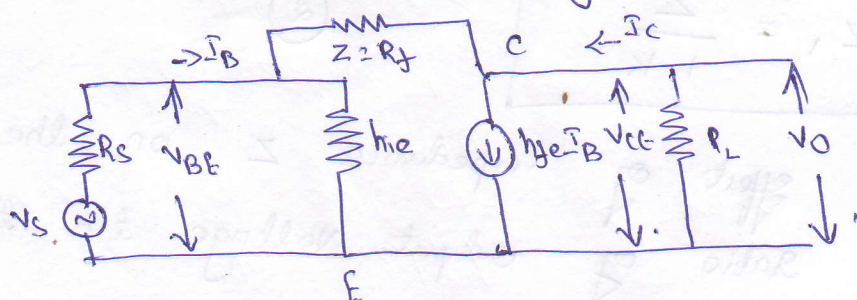
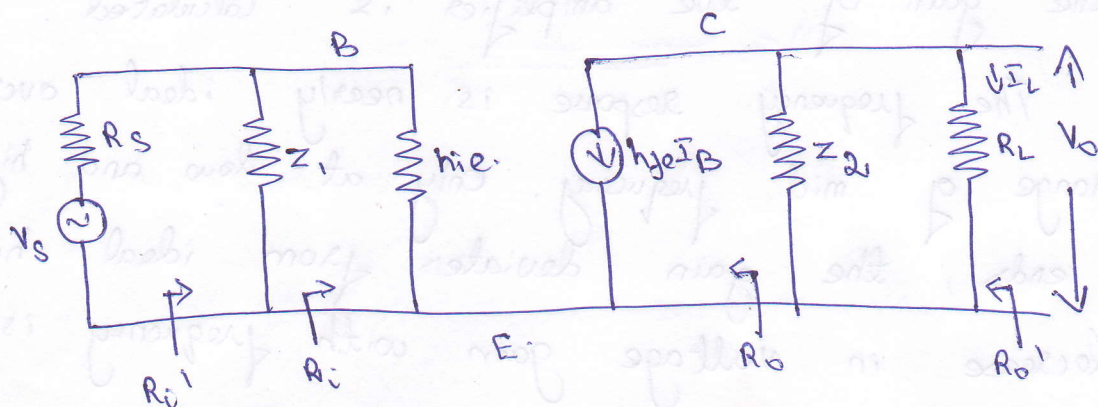


fig. Approximate h-parameter circuit for CE amplifier.

Using millers theorem the approximate model can



be redrawn as



From the approximate model for CE amplifier we can write.

- (i) Current gain  $A_I = -h_{fe}$ .
- (ii) Input resistance  $R_i = h_{ie}$ .
- (iii) Voltage gain  $A_V = \frac{A_I R_o'}{R_i}$

where  $R_o' = Z_2 \parallel R_L$

$$\therefore A_V = \frac{A_I (Z_2 \parallel R_L)}{R_i}$$

- (iv) The output resistance ( $R_o$ ) =  $\infty$ .

Frequency response of an amplifier:-

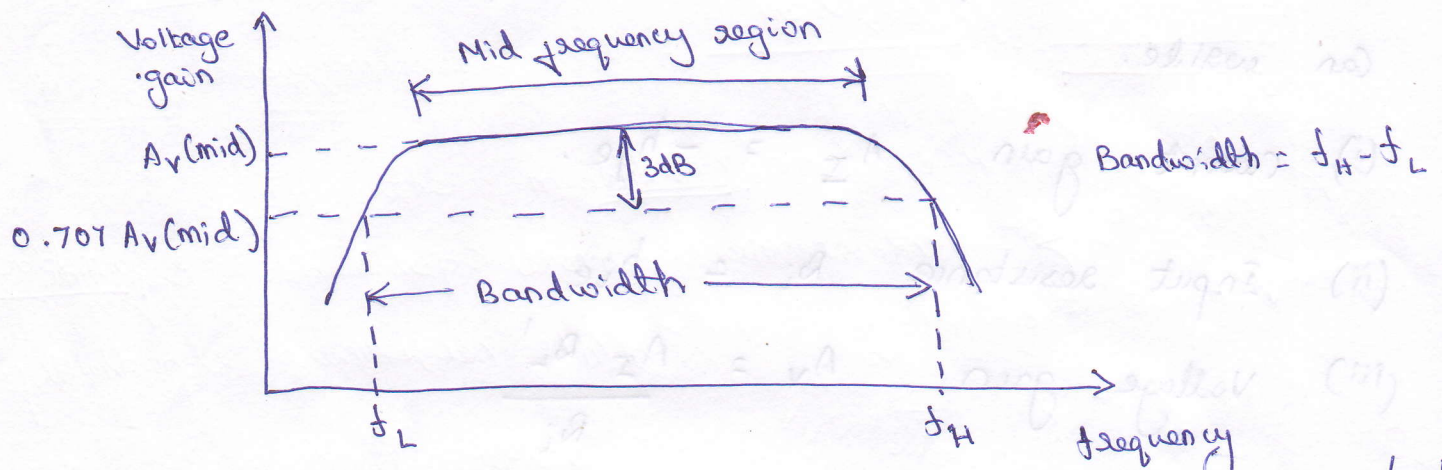
An amplifier should ideally provide the same amplification for all frequencies.

In frequency response curve the input voltage to the amplifier is kept constant and frequency of input signal is continuously varied. Then the output voltage at each frequency of input signal is noted.



and the gain of the amplifier is calculated.

The frequency response is nearly ideal over a wide range of mid frequency. only at low and high frequency ends, the gain deviates from ideal characteristic. The decrease in voltage gain with frequency is called Roll-off.



The two frequencies at which voltage gain starts decreasing below 70.7 % are indicated by  $f_L$  and  $f_H$ . These are called lower cut off and upper cut off frequencies respectively.

These two frequencies are also referred to as half power frequencies since gain (or) output voltage drop to 70.7 % of maximum value and this represents a power level of one half the power at the reference in mid-frequency region.



Problem 4: The voltage amplifier has voltage gain = 200 at cut off frequencies. Find the maximum voltage gain.

Sol:  

$$\text{Max. voltage gain} = \text{Gain at cut off frequency} \times \sqrt{2}$$

$$= 200 \times \sqrt{2}$$

$$= 282.84$$

### Midband Gain:

In the midband, the voltage gain of the amplifier is approximately maximum. It is designated as midband gain (or)  $A_{mid}$ .

The voltage gain of the amplifier circuit outside the midband is approximately given as

$$A = \frac{A_{mid}}{\sqrt{1 + (f_L/f)^2} \sqrt{1 + (f/f_H)^2}}$$

### Midband:-

In the midband,  $f_L/f \approx 0$  and  $f/f_H \approx 0$ , therefore

$$\therefore A = A_{mid}$$

### Below Midband:-

Below the midband,  $f/f_H \approx 0$ . As a result, the equation becomes.

$$A = \frac{A_{mid}}{\sqrt{1 + (f_L/f)^2}}$$

### Above Midband:-

Above midband  $f_L/f = 0$ . As a result, the equation becomes

$$A = \frac{A_{mid}}{\sqrt{1 + (f/f_2)^2}}$$

Problem 5 :- For an amplifier, midband gain = 100 and lower cut off frequency is 1 kHz. Find the gain of an amplifier at frequency 20 Hz.

Solution:-

Below midband  $A = \frac{A_{mid}}{\sqrt{1 + (f/f_2)^2}} = \frac{100}{\sqrt{1 + (1000/20)^2}} = 2$

Problem 6 :- Calculate the transconductance of a MOSFET having following parameters  $V_T = 1V$ ,  $\frac{1}{2} \mu_n C_{ox} = 30 \mu A/V^2$  and  $W/L = 50$ , Assume drain current,  $I_D = 1.2 mA$ .

Solution:-

$$K_n = \left[ \frac{1}{2} \mu_n C_{ox} \right] \left[ \frac{W}{L} \right]$$

$$= \left[ 30 \times 10^{-6} A/V^2 \right] \left[ 50 \right]$$

$$K_n = 1.5 mA/V^2$$

The expression for transconductance.

$$g_m = 2 \sqrt{K_n I_{DQ}} = 2 \sqrt{(1.5 \times 10^{-3}) A/V^2 \times 1.2 \times 10^{-3} A}$$

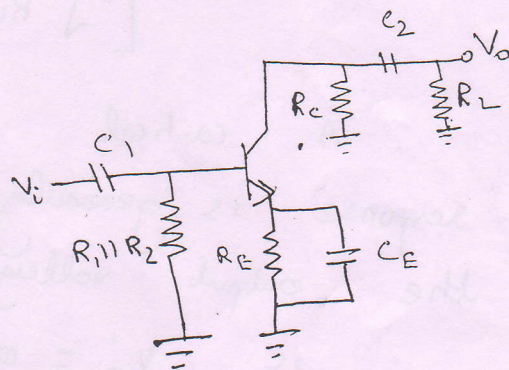
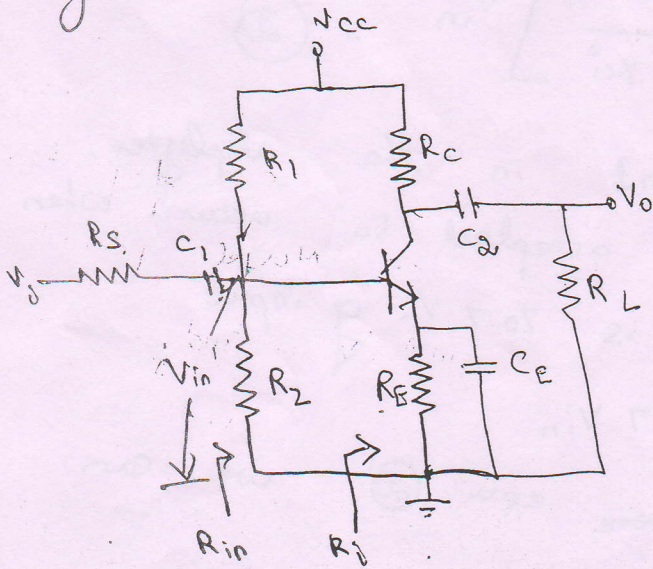
$$g_m = 2.68 mA/V$$



# Frequency Analysis of BJT and MOSFET Amplifier.

## Low frequency response of Amplifier:

At low frequency the reactance of coupling and bypass capacitors become large. So they cannot be neglected.



(a) RC coupled CE amplifier

(b) AC equivalent circuit

The amplifier shown in the fig has three RC networks that affect its gain.

(i) RC network formed by input coupling capacitor  $C_1$  and input impedance of amplifier.

(ii) RC network formed by output coupling capacitor  $C_2$  and resistance at collector.



iii) RC network formed by emitter by pass capacitor  $C_E$  and resistance at emitter.

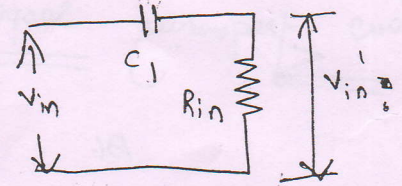
i) Input RC network:

The resistance  $R_{in}$  is given by

$$R_{in} = R_1 \parallel R_2 \parallel h_{ie} \quad \text{--- (1)}$$

Applying voltage divider rule we can write

$$V_{in}' = \left[ \frac{R_{in}}{\sqrt{R_{in}^2 + X_{C1}^2}} \right] V_{in} \quad \text{--- (2)}$$



$$R_{in} = R_1 \parallel R_2 \parallel h_{ie}$$

A critical point in the amplifier response is generally accepted to occur when the output voltage is 70.7% of input i.e.  $V_{in}' = 0.707 V_{in}$

from above equ (2) we can write

$$\frac{V_{in}'}{V_{in}} = \frac{R_{in}}{\sqrt{R_{in}^2 + X_{C1}^2}} = 0.707 = \frac{1}{\sqrt{2}}$$

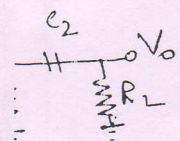
$$\therefore \sqrt{2} R_{in} = \sqrt{R_{in}^2 + X_{C1}^2}$$

Squaring on both side.

$$2 R_{in}^2 = R_{in}^2 + X_{C1}^2$$

$$2 R_{in}^2 - R_{in}^2 = X_{C1}^2$$

$$\boxed{R_{in}^2 = X_{C1}^2}$$



$C_E$

at circuit has three

coupling of

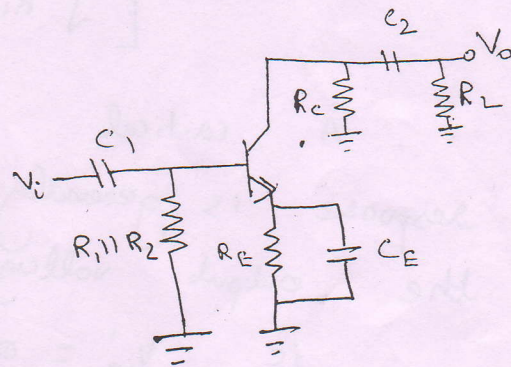
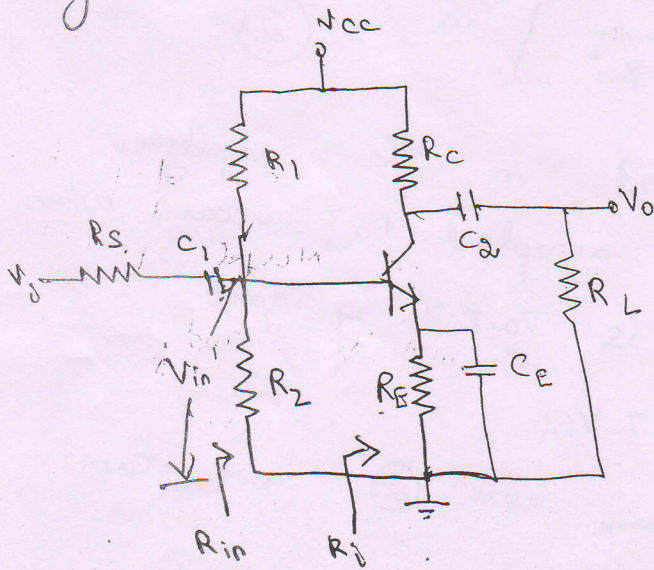
Coupling Collector



# Frequency Analysis of BJT and MOSFET Amplifier.

## Low frequency response of Amplifier:

At low frequency the reactance of coupling and bypass capacitors become large. So they cannot be neglected.



a) RC coupled CE amplifier

(b) AC equivalent circuit

The amplifier shown in the fig has three RC networks that affect its gain.

(i) RC network formed by input coupling capacitor  $C_1$  and input impedance of amplifier.

(ii) RC network formed by output coupling capacitor  $C_2$  and resistance at collector.



will

$$X_{C_1} = \frac{1}{2\pi f_c C_1}$$

Bypass

$$\therefore R_{in} = \frac{1}{2\pi f_c C_1}$$

$V_i$

$R_B$

$T_i$

ie 
$$f_c = \frac{1}{2\pi R_{in} C_1}$$

if the resistance of input source is taken into account then.

the

given

$$f_c = \frac{1}{2\pi (R_s + R_{in}) C_1}$$

Output  $R_C$  network:

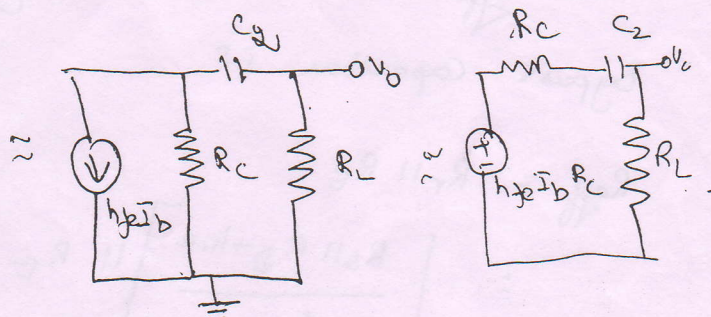
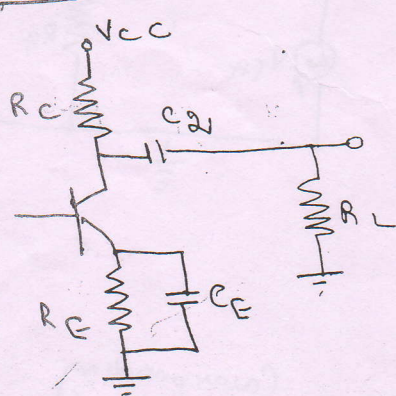


fig. h-parameter equivalent

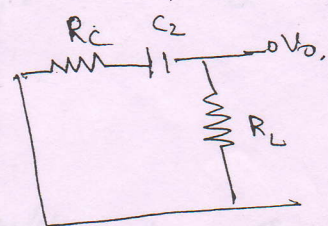
The equivalent resistance is obtained by short-circuiting the voltage source ( $h_{FE} I_B R_C$ ).

bypass

$\therefore$  The equivalent resistance

$R_C$  and  $R_L$  are in series

is



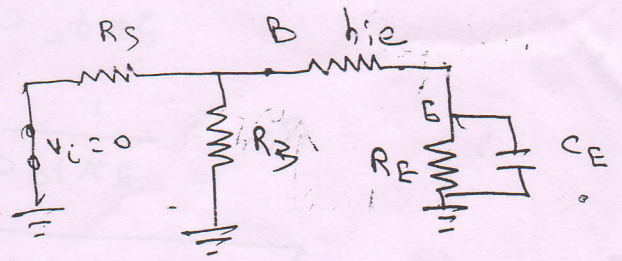
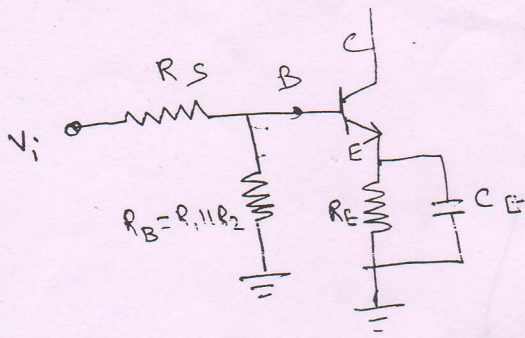
Domino

$$\therefore f_c = \frac{1}{2\pi (R_C + R_L) C_2}$$

frequency network



## Bypass RC Network:



To get the equivalent resistance short circuit the input voltage.

The reflected resistance on emitter side is given by.

$$R_r = \frac{(R_S || R_B) + h_{ie}}{h_{fe}}$$

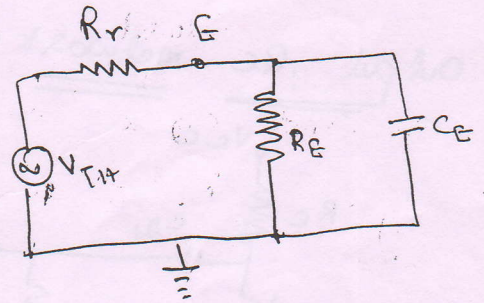
where  $R_B = R_1 || R_2$

$$h_{fe} = \beta$$

The effective resistance seen by bypass capacitor is

$$R_{eff} = R_r || R_E$$

$$= \left[ \frac{R_S || R_B + h_{ie}}{h_{fe}} \right] || R_E$$



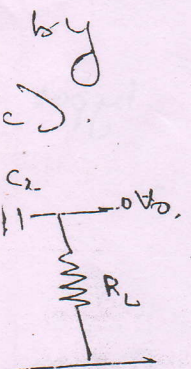
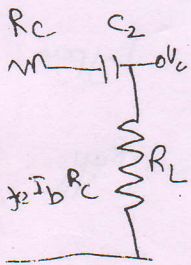
The critical frequency corresponding to bypass capacitor is

$$f_c = \frac{1}{2\pi R_{eff} C_E}$$

## Dominant Network:

The network which has higher critical frequency than other network is called dominant network.

The dominant network determine the





W.K.D

$$X_{C_1} = \frac{1}{2\pi f_c C_1}$$

$$\therefore R_{in} = \frac{1}{2\pi f_c C_1}$$

ie  $f_c = \frac{1}{2\pi R_{in} C_1}$

if the resistance of input source is taken into account then.

$$f_c = \frac{1}{2\pi (R_s + R_{in}) C_1}$$

Output  $R_C$  network:

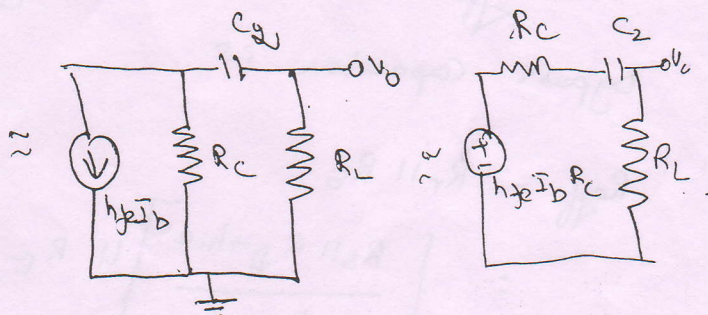
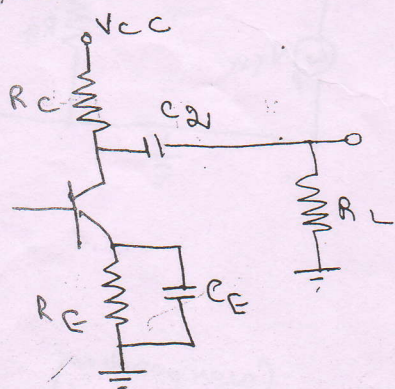


fig. 4 - parameter equivalent

The equivalent resistance is obtained by short circuiting the voltage source ( $h_{fe} I_B R_C$ ).

$\therefore$  The equivalent resistance

is  $R_C$  and  $R_L$  are in series

$$\therefore f_c = \frac{1}{2\pi (R_C + R_L) C_2}$$

Bypass

$V_i$

$R_E$

$T_i$

the

given

The

bypass

$R_{eff}$

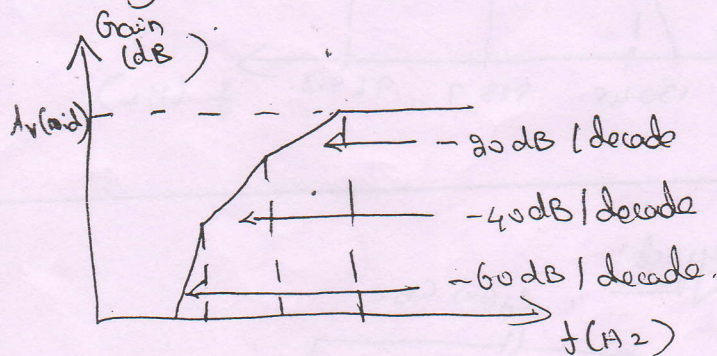
bypass

Domino

frequency network



frequency at which the overall gain of an amplifier begin to drop at  $-20 \text{ dB/decade}$ .



low frequency response of RC coupled

Problem:

Calculate the cut-off frequency due to  $C_1$  and  $C_2$  &  $C_E$  in the circuit shown below  
 given  $h_{fe} = 100$ ,  $h_{ie} = 3 \text{ k}\Omega$  ~~1.1 k~~

a) Input RC Network

$$f_c = \frac{1}{2\pi [R_s + (R_1 \parallel R_2 \parallel h_{ie})] C_1}$$

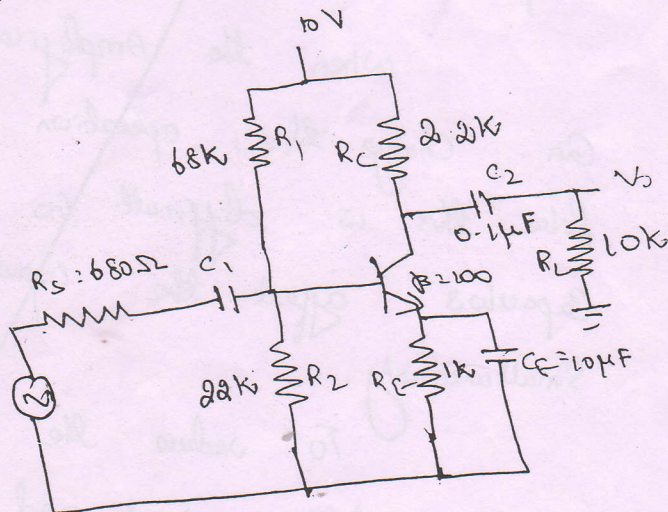
$$= 989.8 \text{ Hz}$$

b) o/p RC Network

$$f_c (\text{output}) = \frac{1}{2\pi (R_c \parallel R_L) C_2} = 130.45 \text{ Hz}$$

c) Bypass RC Network

$$f_c = \frac{1}{2\pi \left[ \left( \frac{R_{eq} + h_{ie}}{h_{fe}} \right) \parallel R_E \right] C_E} = 923.7 \text{ Hz}$$



$C_1$   
amp.  
input

Can  
like  
Capacit  
Small

exists  
theorem

— Connec  
into



Small Signal Parameters:

The instantaneous gate to source voltage is.

$$V_{GS} = \cancel{V_{GSQ}} + V_i = V_{GSQ} + v_{gs} \quad \dots (1)$$

where  $V_{GSQ}$  is d.c component  
 $v_{gs}$  is ac. component

The instantaneous drain current is

$$i_D = K_n (V_{GS} - V_T)^2 \quad \dots (2)$$

Sub eqn (1) in (2) we get.

$$i_D = K_n [(V_{GSQ} + v_{gs}) - V_T]^2$$

$$i_D = K_n [(V_{GSQ} - V_T) + v_{gs}]^2$$

$$i_D = \underbrace{K_n (V_{GSQ} - V_T)^2}_{\text{DC component}} + \underbrace{2K_n v_{gs} (V_{GSQ} - V_T)}_{\text{Time Varying } i_D \text{ Component}} + \underbrace{K_n v_{gs}^2}_{\text{Produce harmonics}} \quad (3)$$

For sinusoidal input signal, the squared term produce undesirable harmonics. To minimize these harmonics we must have

$$v_{gs} \ll 2(V_{GSQ} - V_T)$$



neglecting the  $v_{gs}^2$  term we can write  
 eqn (3) as

$$i_D = k_n (V_{GS0} - V_T)^2 + 2k_n (V_{GS0} - V_T) v_{gs}$$

let us assign.

$$I_{D0} = k_n (V_{GS0} - V_T)^2$$

$$i_d = 2k_n (V_{GS0} - V_T) v_{gs}$$

$$\therefore i_D = I_{D0} + i_d$$

The small signal drain current is related  
 to the small signal gate to source voltage  
 by transconductance  $g_m$ .

$$g_m = \frac{i_d}{v_{gs}} = \frac{2k_n (V_{GS0} - V_T) v_{gs}}{v_{gs}}$$

$$g_m = 2k_n (V_{GS0} - V_T) \quad \text{--- (5)}$$

(or)

$$g_m = \frac{\partial i_d}{\partial v_{gs}} = 2k_n (V_{GS0} - V_T)$$

$$g_m = 2k_n (V_{GS0} - V_T)$$

The above eqn can be rewritten as

$$g_m = 2 \sqrt{k_n I_{D0}}$$

(6)

$v_n v_{gs}^2$  (3)

Produce  
 harmonics

Squared  
 to

have



Small Signal equivalent circuit:

from the circuit diagram of n-channel MOSFET. the o/p voltage.

$$V_o = V_{DD} - i_D R_D \quad \dots (7)$$

Sub eqn (4) in eqn (7) we get.

$$\begin{aligned} V_{io} &= V_{DD} - (I_{DQ} + i_d) R_D \\ &= V_{DD} - I_{DQ} R_D - i_d R_D \quad \dots (8) \end{aligned}$$

The time varying drain to source voltage is equal to  $v_o$  and it is given by.

$$v_o = v_{ds} = -i_d R_D$$

w.k.t  $i_d = g_m v_{gs}$

in short we can write.

$$\begin{aligned} v_{ds} &= -i_d R_D \equiv \cancel{I_D} = g_m v_{gs} \\ i_d &= g_m v_{gs} = \cancel{I_D} \end{aligned}$$

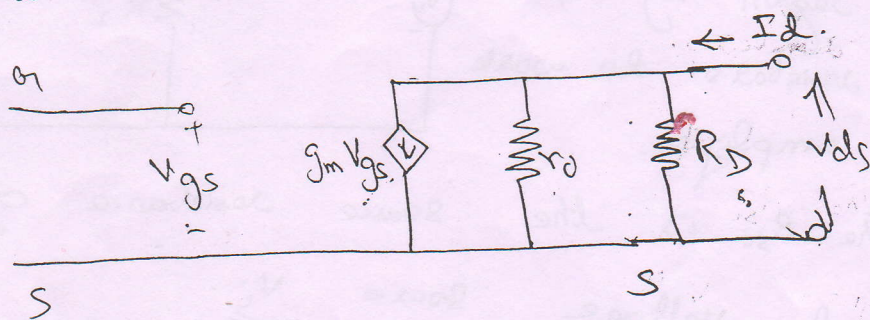
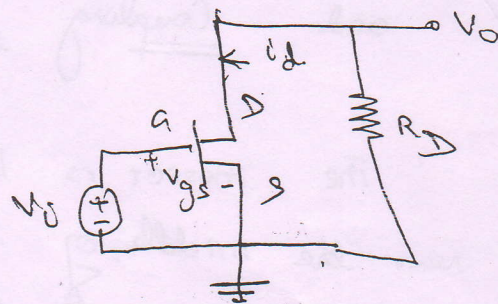
$$\begin{cases} v_{ds} = -i_d R_D \equiv V_{ds} = -I_D R_D \\ i_d = g_m v_{gs} \equiv I_d = g_m v_{gs} \end{cases}$$



not  
various

The ac equivalent circuit of enhanced MOSFET is shown below where dc source is made zero.

The below figure shows the small signal low frequency ac equivalent circuit for n-channel MOSFET.



8)

Voltage

by

Due to non zero slope in  $i_D$  versus  $v_{DS}$  curve we have.

$$i_D = K_n [(v_{GS} - V_T)^2 (1 + \lambda v_{DS})] \quad \text{--- (1)}$$

The small signal o/p resistance is given by.

$$r_o = \left( \frac{\partial i_D}{\partial v_{DS}} \right)^{-1} \Big|_{v_{GS} = V_{GS} = \text{const.}}$$

differentiate eqn (1) w.r.t.  $v_{DS}$

we get.

$$i_D = [K_n \lambda (v_{GS} - V_T)^2]^{-1} \quad \text{from eqn (1)}$$

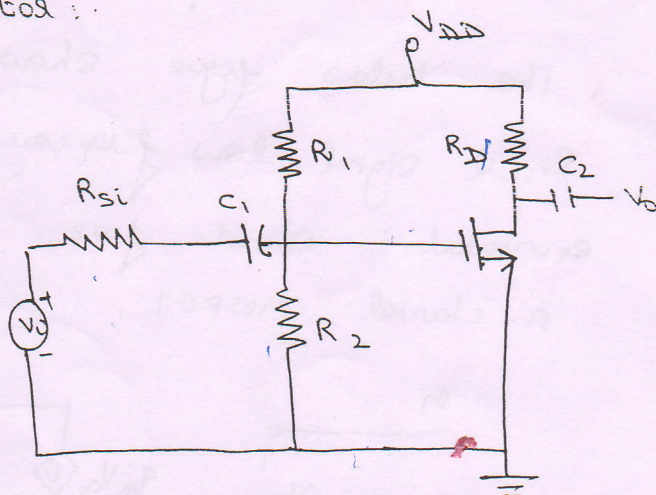
$r_o = [\lambda I_{DQ}]^{-1}$



# Common Source Amplifier:

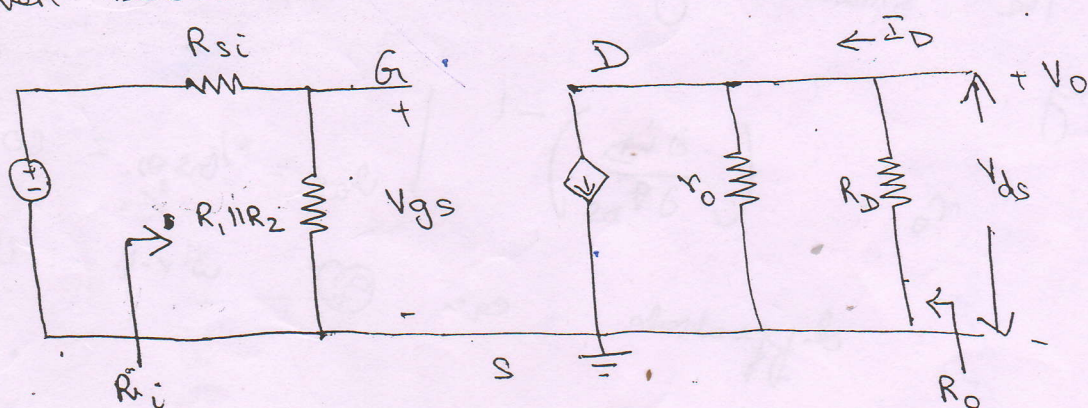
Common Source Circuit with voltage divider biasing and Coupling Capacitor:

The MOSFET is biased near the middle of the saturation region by  $R_1$  and  $R_2$  resistors to work as an amplifier.



The  $R_{si}$  is the source resistance of the signal voltage source  $V_i$ .  $R_{si}$  should be much less than the amplifier input resistance,  $R_i = R_1 || R_2$  in order to minimize loading effect.

The small signal equivalent circuit is given below.



The input gate to source voltage is given as,

$$V_{gs} = \left[ \frac{R_o}{R_i + R_{si}} \right] V_i \quad \text{--- (1)}$$

$$\therefore V_i = \frac{V_{gs}}{\frac{R_o}{R_i + R_{si}}}$$

Step 1:

Step 2:



making  
zero

$$R_i = R_1 || R_2 = 82 || 30 = 21.96 \text{ k}\Omega$$

$$A_v = -g_m (r_o || R_o) \left[ \frac{R_i}{R_i + R_{si}} \right]$$

the

$$A_v = -7.55$$

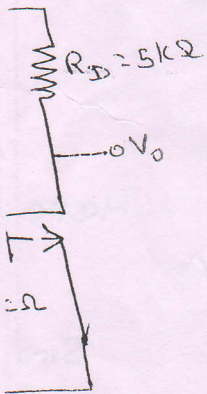
$$0.8 \text{ mA/V}^2$$

gain

$$R_o = R_D || r_o = 5 || 90 = 4.737 \text{ k}\Omega$$

Common source amplifier with source resistor

$$V_D = 10 \text{ V}$$



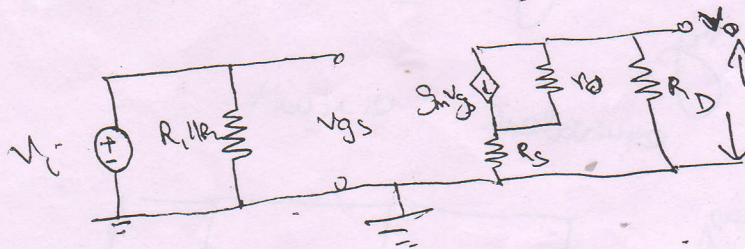
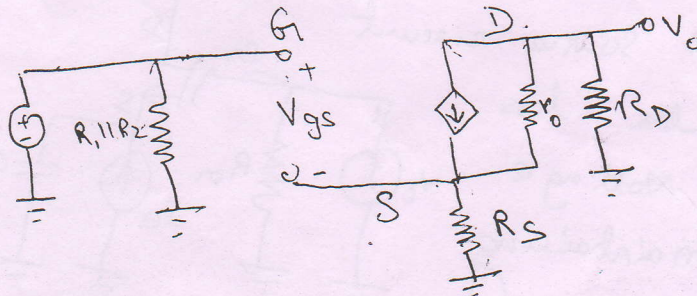
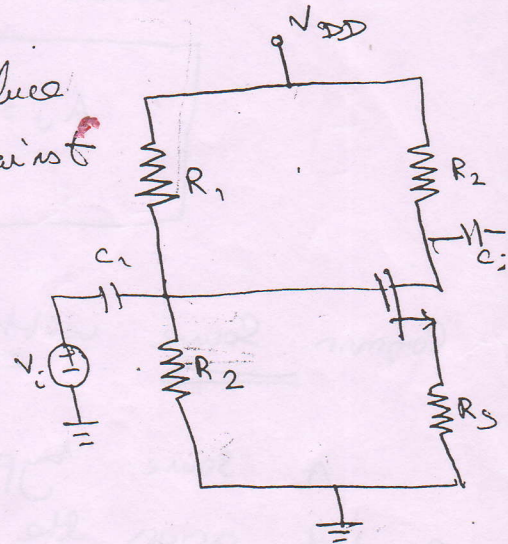
$$I_D = 1.11 \text{ mA}$$

$$V_{GS} = 4.5 \text{ V}$$

let

The source resistor is introduced to stabilize the Q-point against variation in the MOSFET parameters

The small signal equivalent is shown below



To find  $A_v$ :

$$v_o = -g_m v_{gs} (R_D || r_o)$$

Apply KVL equation from input to gate -  
Source loop.

$$\text{mA/V}$$

$$-1$$



$$V_i = V_{gs} + (g_m V_{gs})(R_S \parallel r_o) \quad (2)$$

$$\therefore A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs} R_D}{V_{gs}(1 + g_m R_S \parallel r_o)}$$

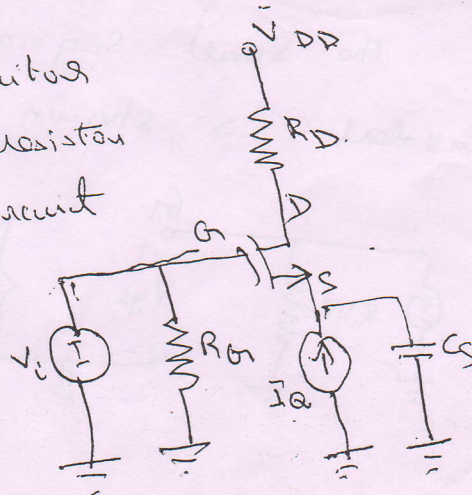
$$A_v = \frac{-g_m R_D}{1 + g_m(R_S \parallel r_o)}$$

when  $r_o \gg R_S$

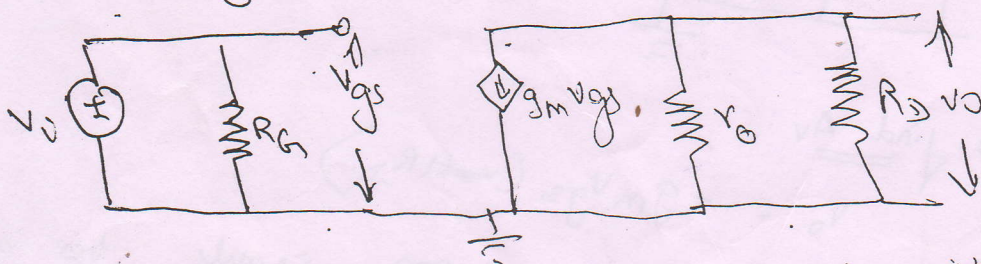
$$\therefore A_v = \frac{-g_m R_D}{1 + g_m R_S}$$

### Common Source with Source Bypass Capacitor

A source bypass capacitor connected across the source resistor in the common-source circuit will minimize the loss in the signal voltage gain, while maintaining Q-point stability.



Small signal equivalent circuit.



from the ~~circuit~~ Small signal equivalent circuit.

MOSFET

Small

of voltage show



$V_i$



$$V_i = V_{gs} \quad \text{--- (1)}$$

$$V_o = -g_m V_{gs} (r_o \parallel R_D)$$

$$\therefore A_v = \frac{V_o}{V_i} = \frac{-g_m \cancel{V_{gs}} (r_o \parallel R_D)}{\cancel{V_{gs}}}$$

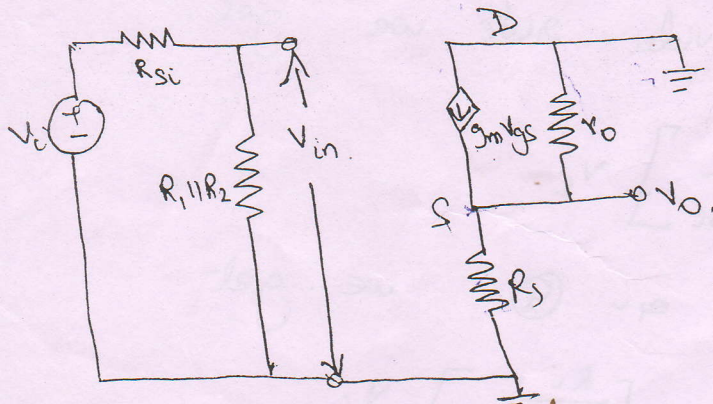
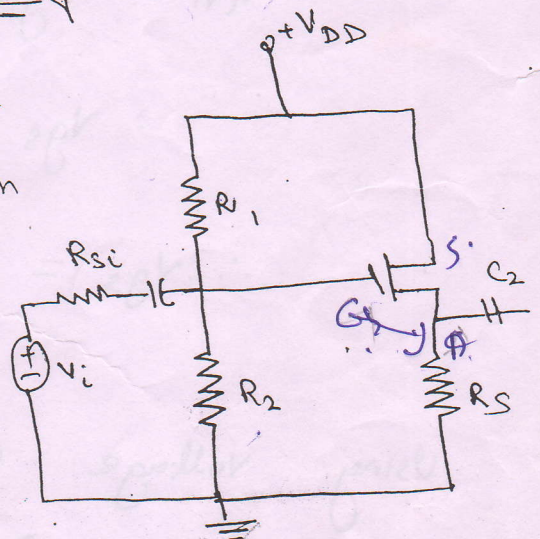
$$A_v = -g_m (r_o \parallel R_D)$$

when  $r_o \gg R_D$

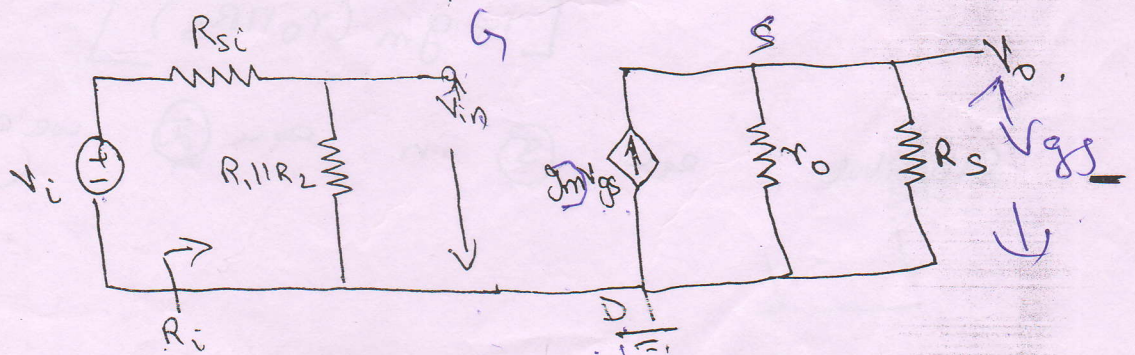
$$\therefore A_v = -g_m R_D$$

MOSFET Source follower Amplifier [Common Drain]

Small signal equivalent circuit  
of MOSFET source follower in  
voltage divider bias is  
shown below.



Small signal equivalent circuit.





Input resistance: ( $R_i$ )

$$R_i = R_1 \parallel R_2 \quad \dots (1)$$

Voltage gain: ( $A_v$ )

$$V_o = g_m V_{gs} (r_o \parallel R_s) \quad \dots (2)$$

Applying KVL to the outer loop we get.

$$V_{in} = V_{gs} + V_o \quad \dots (3)$$

Substitute eqn (2) in (3) we get.

$$\begin{aligned} V_{in} &= V_{gs} + g_m V_{gs} (r_o \parallel R_s) \\ &= V_{gs} [1 + g_m (r_o \parallel R_s)] \end{aligned}$$

$$\therefore V_{gs} = \frac{V_{in}}{[1 + g_m (r_o \parallel R_s)]} \quad \dots (4)$$

Using voltage divider rule we get.

$$V_{in} = \left[ \frac{R_i}{R_i + R_{sc}} \right] V_c$$

Sub  $V_{in}$  in eqn (4) we get.

$$V_{gs} = \frac{\left[ \frac{R_i}{R_i + R_{sc}} \right] V_i}{[1 + g_m (r_o \parallel R_s)]} \quad \dots (5)$$

Substitute eqn (5) in eqn (2) we get



Mos

Nmos

to

Input

Voltage



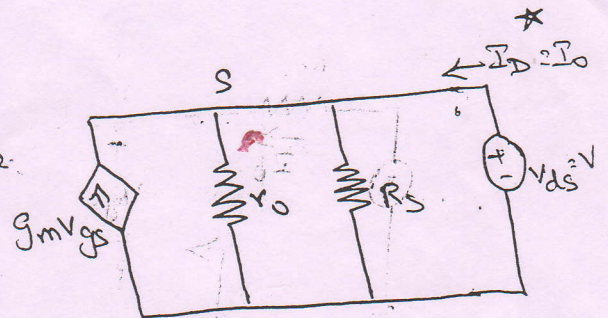
$$V_o = g_m (r_{o1} \parallel R_s) \left[ \left( \frac{R_i}{R_i + R_{s1}} \right) V_i \left( \frac{1}{1 + g_m (r_{o1} \parallel R_s)} \right) \right]$$

rearrange the above equation we get.

$$A_v = \frac{V_o}{V_i} = \frac{g_m (r_{o1} \parallel R_s)}{(1 + g_m (r_{o1} \parallel R_s))} \left( \frac{R_i}{R_i + R_{s1}} \right) \quad (6)$$

Output resistance ( $R_o$ ) :

Apply KCL to the o/p node we get.



$$I_D + g_m V_{gs} = \frac{V_{ds}}{r_o} + \frac{V_{ds}}{R_s} \quad (7)$$

when input current is zero. from eqn (3).

$$V_{gs} = -V_{ds} \quad (8)$$

sub (8) in (7) we get.

$$I_D - g_m V_{ds} = \frac{V_{ds}}{r_o} + \frac{V_{ds}}{R_s}$$

$$I_D = \frac{V_{ds}}{r_o} + \frac{V_{ds}}{R_s} + g_m V_{ds}$$

$$I_D = V_{ds} \left[ \frac{1}{r_o} + \frac{1}{R_s} + \frac{1}{(1/g_m)} \right]$$

$$R_o = \frac{V_{ds}}{I_D} = \frac{1}{\left[ \frac{1}{r_o} + \frac{1}{R_s} + \frac{1}{g_m} \right]}$$

$$R_o = r_o \parallel R_s \parallel \frac{1}{g_m}$$



## Internal Capacitance of MOSFET and high frequency model:

There are two types of internal capacitance in MOSFET namely.

### i) Gate Capacitance:-

It is a parallel plate capacitance formed by a gate electrode with the channel, with the oxide layer act as a capacitor dielectric. It is denoted as  $C_{ox}$ .

### ii) Junction Capacitance:-

These capacitance are due to the reverse-biased pn junction formed by  $n^+$  source region and p-type substrate and  $n^+$  drain region and p-type substrate. These are denoted as source diffusion and drain diffusion capacitance respectively.

### Values of gate capacitance:-

In triode region, the channel length has uniform depth and hence we have.

$$C_{gs} = C_{gd} = \frac{1}{2} WL C_{ox} \quad [\text{Triode region}]$$

In saturation region, the channel has a tapered shape and is pinched off at  $(x)$  near the drain.

$$\left. \begin{aligned} C_{gs} &= \frac{2}{3} WL C_{ox} \\ C_{gd} &= 0 \end{aligned} \right\} [\text{Saturation region}]$$



In cut off region, the channel disappears and

$$C_{gs} = C_{gd} = 0 \quad [\text{cut off}]$$

The gate-body model capacitance is given by.

$$C_{gb} = WL C_{ox} [\text{cutoff}]$$

Due to the fact that the source and drain diffusions extend slightly under the gate oxide we need to add the capacitive component ( $C_{ov}$ ) to the  $C_{gs}$  and  $C_{gd}$  in the above function.

$$\text{Overlap Capacitance } [C_{ov}] = WL_{ov} \cdot C_{ox}$$

a) Junction Capacitance:-

Source diffusion capacitance is given by.

$$C_{sb} = \frac{C_{sbo}}{\sqrt{1 + \frac{V_{SB}}{V_0}}}$$

where,  $C_{sbo}$  - is value of  $C_{sb}$  at zero body-source bias.

$V_{SB}$  - Magnitude of reverse-bias voltage.

$V_0$  - Junction built-in voltage.

Similarly drain diffusion capacitance is -

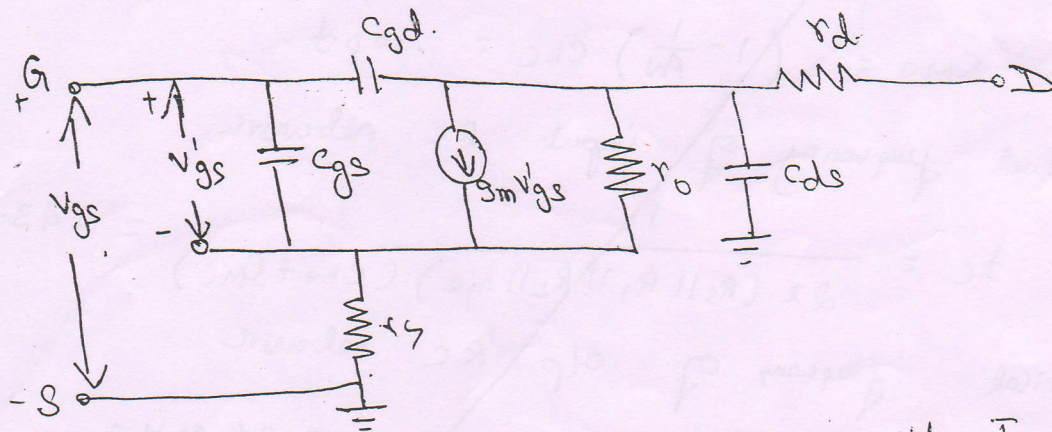
$$C_{db} = \frac{C_{dbo}}{\sqrt{1 + \frac{V_{DB}}{V_0}}} //$$







The Small Signal equivalent circuit for the n-channel Common-Source MOSFET is shown below



The parameter  $r_o$  is related with  $I_D$  versus  $V_{DS}$ . For ideal MOSFET biased in the saturation region,  $I_D$  is independent of  $V_{DS}$ , hence  $r_o$  is infinite.

Source resistance  $r_s$  have a significant effect on transistor characteristic frequency, equivalent circuit including  $r_s$  but not  $r_o$ .

for the circuit shown, the drain current is

$$I_d = g_m V'_{gs}$$

The relationship between  $V_{gs}$  and  $V'_{gs}$  is

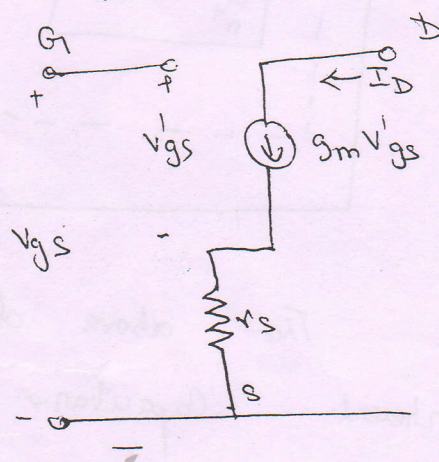
$$V_{gs} = V'_{gs} + (g_m V'_{gs}) r_s$$

$$V_{gs} = V'_{gs} [1 + g_m r_s]$$

$$\therefore V'_{gs} = \frac{V_{gs}}{[1 + g_m r_s]}$$

Sub  $V'_{gs}$  in  $I_d$  we get

$$I_d = \frac{g_m}{[1 + g_m r_s]} V_{gs} = g_m' V_{gs} //$$

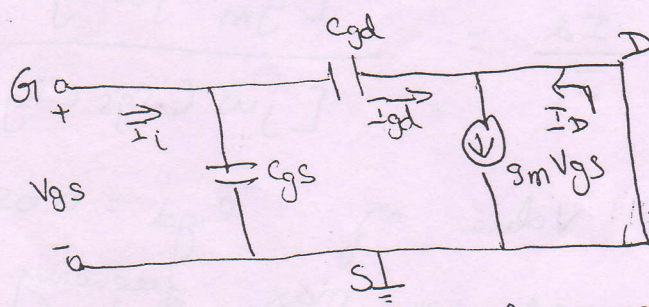




## MOSFET UNITY - GAIN FREQUENCY:-

It is defined as the frequency at which the short-circuit current gain of the common source configuration becomes unity.

If  $r_s, r_d, r_o$ , and  $C_{ds}$  are neglected and connected drain to signal ground, the resulting small signal circuit is shown below.



Apply KCL at input node we get:

$$I_i = \frac{V_{gs}}{\left(\frac{1}{j\omega C_{gs}}\right)} + \frac{V_{gs}}{\left(\frac{1}{j\omega C_{gd}}\right)} \quad \text{--- (1)}$$

$$= j\omega C_{gs} V_{gs} + j\omega C_{gd} V_{gs}$$

$$I_i = j\omega V_{gs} [C_{gs} + C_{gd}] \quad \text{--- (2)}$$

Similarly apply KCL at output node we get

$$\frac{V_{gs}}{\frac{1}{j\omega C_{gd}}} + I_D = g_m V_{gs} \quad \text{--- (3)}$$

$$j\omega V_{gs} C_{gd} + I_D = g_m V_{gs}$$

$$I_D = g_m V_{gs} - j\omega V_{gs} C_{gd}$$

$$= V_{gs} [g_m - j\omega C_{gd}]$$



$$\therefore V_{gs} = \frac{-I_d}{[g_m - j\omega C_{gd}]} \quad \text{--- (4)}$$

Substitute eqn (4) in (2) we get

$$I_i = \frac{I_d [j\omega (C_{gs} + C_{gd})]}{[g_m - j\omega C_{gd}]}$$

$$A_I = \frac{I_d}{I_i} = \frac{[g_m - j\omega C_{gd}]}{[j\omega (C_{gs} + C_{gd})]} \quad \text{--- (5)}$$

If typical value of  $C_{gd} = 0.05 \text{ pF}$  and  $f = 100 \text{ MHz}$   
 $g_m = 1 \text{ mA/V}$  assumed for max frequency

$$\omega C_{gd} \ll g_m$$

$\therefore$  eqn (5) become

$$A_I \approx \frac{g_m}{[j\omega (C_{gs} + C_{gd})]} \quad \text{--- (6)}$$

for unit gain  $A_I = 1$  and  $f = f_T$

$$1 = \frac{g_m}{[2\pi f_T (C_{gs} + C_{gd})]}$$

$$\therefore f_T = \frac{g_m}{2\pi [C_{gs} + C_{gd}]}$$

adling  
freque





PROBLEM:

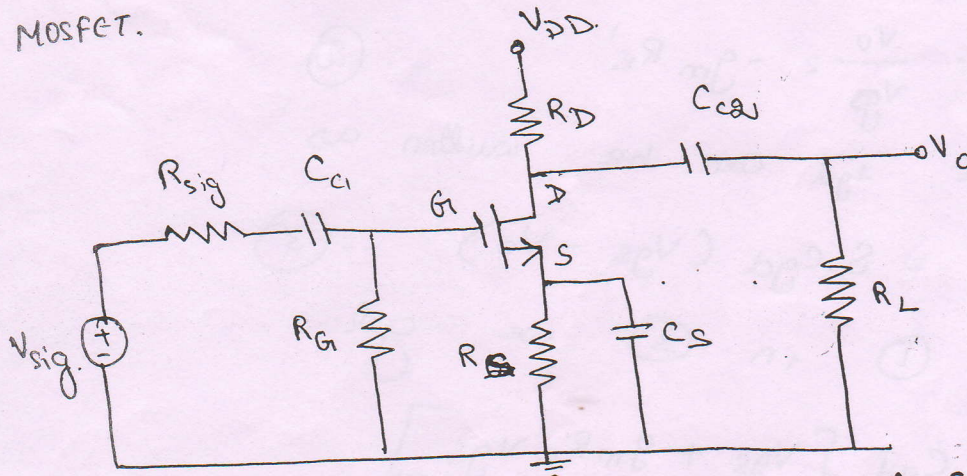
Determine the unity gain bandwidth of MOSFET. The transistor parameters are  $k_n = 0.25 \text{ mA/V}^2$ ,  $V_{TN} = 1 \text{ V}$ ,  $\lambda = 0$ ,  $C_{gd} = 0.04 \text{ pF}$  and  $C_{gs} = 0.2 \text{ pF}$  and assume  $V_{gs} = 3 \text{ V}$ .

Sol:-

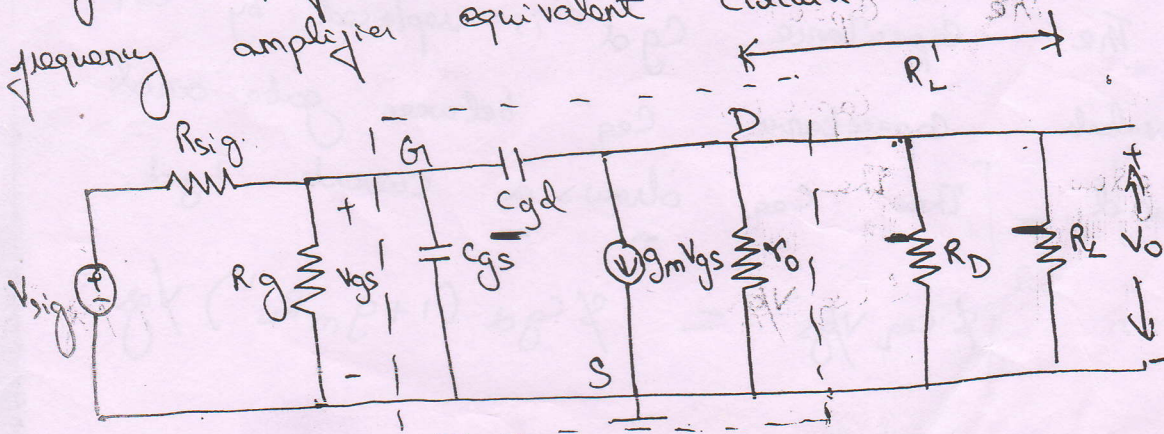
$$g_m = 2k_n (V_{gs} - V_T) = 1 \text{ mA/V}$$

$$f_T = \frac{g_m}{2\pi [C_{gs} + C_{gd}]} = 663 \text{ MHz}$$

High frequency response of MOSFET CS AMPLIFIER. To determine the gain of the amplifier at high frequency and upper 3-dB frequency, consider the high frequency model of MOSFET.

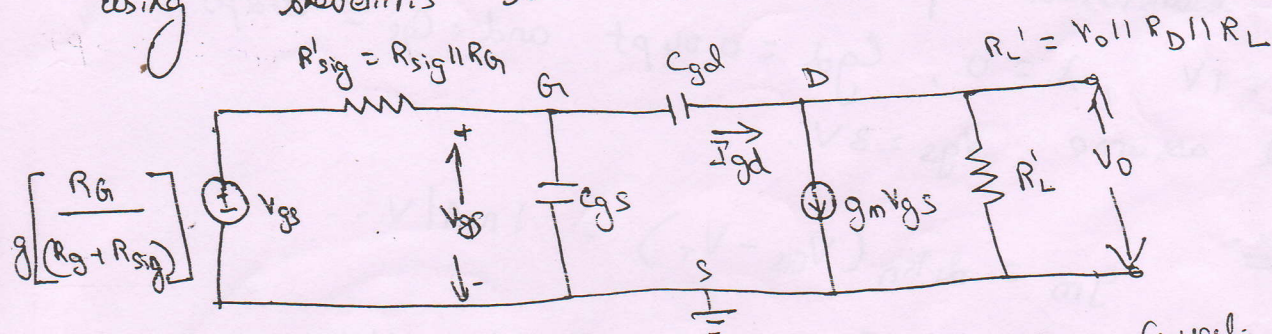


At high frequency  $C_{c1}$ ,  $C_{c2}$  and  $C_S$  will be acting as perfect short circuit. The resultant high frequency amplifier equivalent circuit is shown below.





The equivalent circuit can be simplified by using Thevenin's theorem as shown below.



Consider first the o/p node. The load current is  $(g_m V_{gs} - I_{gd})$  where  $g_m V_{gs}$  is o/p current of transistor.

The current  $I_{gd}$  is the current supplied through the very small capacitance  $C_{gd}$ . But  $I_{gd} < g_m V_{gs}$ .

$$\therefore V_o = -(g_m V_{gs}) R'_L = -g_m R'_L V_{gs} \quad \text{--- (1)}$$

$$\therefore \frac{V_o}{V_{gs}} = -g_m R'_L \quad \text{--- (2)}$$

The current  $I_{gd}$  can be written as

$$I_{gd} = s C_{gd} (V_{gs} - V_o) \quad \text{--- (3)}$$

sub eqn (1) in (3) we get

$$\begin{aligned} I_{gd} &= s C_{gd} [V_{gs} + g_m R'_L V_{gs}] \\ &= s C_{gd} V_{gs} [1 + g_m R'_L] \quad \text{--- (4)} \end{aligned}$$

The capacitance  $C_{gd}$  is replaced by an equivalent capacitance  $C_{eq}$  between gate and ground. The  $C_{eq}$  draws a current  $I_{gd}$ .

$$\therefore s C_{eq} V_{gs} = s C_{gd} (1 + g_m R'_L) V_{gs}$$

$$\left( \frac{R_G}{R_G + R_{sig}} \right)'$$

I  
of  
can

wh

u

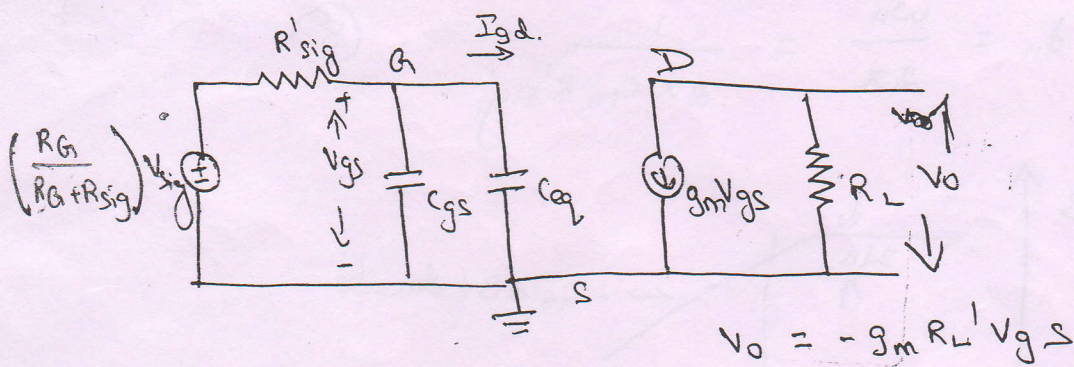
sub

mid bc



$$\therefore C_{eq} = C_{gd} (1 + g_m R_L') \quad \dots (5)$$

$\therefore$  The circuit can be redrawn as



The above circuit is single time constant (STC) of low pass type. The o/p voltage  $V_o$  of STC can be expressed as

$$V_{gs} = \left[ \frac{R_G}{R_G + R_{sig}} \right] V_{sig} \cdot \frac{1}{1 + \frac{s}{\omega_0}} \quad \dots (6)$$

where  $\omega_0$  is the break frequency of STC circuit

$$\omega_0 = \frac{1}{C_{in} R'_{sig}} \quad \dots (7)$$

where  $C_{in} = C_{gs} + C_{eq}$

$$C_{in} = C_{gs} + C_{gd} (1 + g_m R_L')$$

$$R'_{sig} = R_{sig} \parallel R_G$$

Substitute from eqn (6) in eqn (1) we get.

$$\frac{V_o V_{gs}}{V_{sig}} = - \left[ \frac{R_G}{R_G + R_{sig}} \right] (g_m R_L') \frac{1}{1 + \frac{s}{\omega_0}}$$

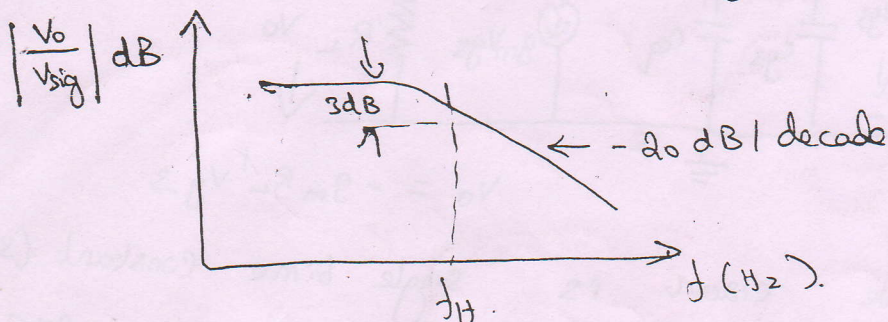
Let as assign  $A_m = - \left[ \frac{R_G}{R_G + R_{sig}} \right] (g_m R_L')$  is mid band gain.

$$\therefore \frac{V_o}{V_{sig}} = \frac{A_m}{1 + \frac{s}{\omega_0}} \quad \dots (7)$$



$$\omega_H = \omega_0 = \frac{1}{C_{in} R'_{sig}} \text{ is upper 3 dB frequency.}$$

$$\text{and } f_H = \frac{\omega_H}{2\pi} = \frac{1}{2\pi C_{in} R'_{sig}} \quad (8)$$



Problem:

Find the mid band gain  $A_m$  and upper 3-dB frequency  $f_H$  of a CS amplifier. Neglect with a signal source having an internal resistance  $R_{sig} = 100 \text{ k}\Omega$ . The amplifier has  $R_G = 4.7 \text{ M}\Omega$ ,  $R_D = R_L = 15 \text{ k}\Omega$ ,  $g_m = 1 \text{ mA/V}$ ,  $r_o = 150 \text{ k}\Omega$ ,  $C_{gs} = 1 \text{ pF}$  and  $C_{gd} = 0.4 \text{ pF}$ .

Sol:

$$A_m = \frac{-R_G}{R_G + R_{sig}} g_m R'_L = -7$$

$$\text{where } R'_L = r_o \parallel R_D \parallel R_L$$

$$C_{eq} = (1 + g_m R'_L) C_{gd} = 3.26 \text{ pF}$$

$$C_{in} = C_{gs} + C_{eq} = 4.26 \text{ pF}$$

$$f_H = \frac{1}{2\pi C_{in} (R_{sig} \parallel R_G)} = 38.2 \text{ kHz}$$

The is.

i) Inp

(ii) Out



## UNIT - IV

### MULTISTAGE AMPLIFIERS AND DIFFERENTIAL AMPLIFIER

#### Multi stage Amplifier:-

An amplifier should have a desired voltage gain & current gain and it should match its input impedance of source with output impedance of loads. but with single stage amplifier this cannot be achieved.

Therefore more than one amplifier stages are cascaded. So that the input and output stages provide impedance matching requirement with some amplification and remaining middle stages provide most of the amplification.

#### Limitations of Multi stage Amplifier:-

1. The bandwidth of multistage amplifier is always less than that of bandwidth of single stage amplifier.
2. Non linear distortion is more in multistage amplifier than single stage amplifier.

#### Two stage Cascaded Amplifier:-

The block diagram of two stage cascaded amplifier is shown below next page. The stages are connected such that the output of the first stage is connected to the input of the second stage.



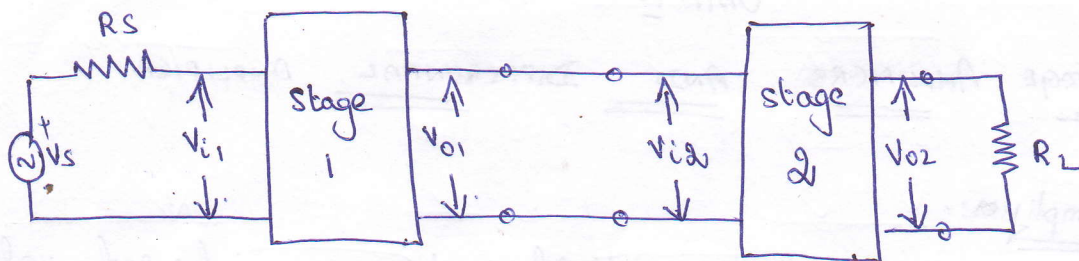


Fig. Block diagram of two stage cascade amplifier.

In the above block diagram  $V_{i1}$  is the input of the first stage and  $V_{o2}$  is the output of second stage. The overall voltage gain of the two stage cascade amplifier can be written as

$$A_v = \frac{V_{o2}}{V_{i1}} = \frac{V_{o2}}{V_{i2}} \times \frac{V_{i2}}{V_{i1}} \quad \dots (1)$$

where as  $V_{o1} = V_{i2}$ .

$$\therefore A_v = \frac{V_{o2}}{V_{i2}} \times \frac{V_{o1}}{V_{i1}} = A_{v2} \cdot A_{v1}$$

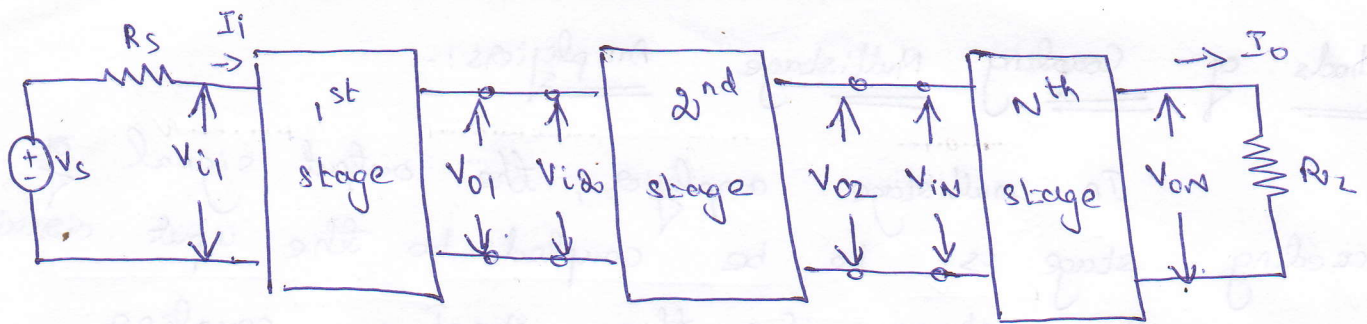
$$\therefore A_v = A_{v2} \cdot A_{v1} \quad \dots (2)$$

From the above expression the voltage gain of multistage amplifier is the product of voltage gain of individual stages.

N-stage Cascaded Amplifier:-

The block diagram of n-stage cascaded voltage amplifier is shown below. where the overall voltage gain is

$$A_v = A_{v1} \times A_{v2} \times A_{v3} \times \dots \times A_{vN} \quad \dots (3)$$



Gain  $\nabla$  Multistage Amplifier:

Gain of an amplifier are represented in terms of decibel, (dB). It is given as

$$N = 10 \log_{10} \left( \frac{\text{Output Power}}{\text{Input Power}} \right)$$

The gain of a multistage amplifier can be easily calculated if the gain of the individual stages are known in dB.

$$20 \log_{10} A_v = 20 \log_{10} A_{v1} + 20 \log_{10} A_{v2} + \dots + 20 \log_{10} A_{vN}$$

$$A_v(\text{dB}) = A_{v1}(\text{dB}) + A_{v2}(\text{dB}) + \dots + A_{vN}(\text{dB})$$

PROBLEM 1:- If the voltage gain of the amplifier is 100, calculate its gain on dB scale.

Sol:-

$$\text{Gain in dB} = 20 \log_{10} [100] = 20 \times 2 = 40 \text{ dB}$$

PROBLEM 2:- Two amplifiers, having gain 20dB and 40dB are cascaded. Find the overall gain in dB.

$$A_v(\text{dB}) = A_{v1}(\text{dB}) + A_{v2}(\text{dB})$$

$$= 20 \text{ dB} + 40 \text{ dB}$$

$$A_v(\text{dB}) = 60 \text{ dB} //$$



## Methods of Coupling Multistage Amplifiers:-

In multistage amplifier, the output signal of preceding stage is to be coupled to the input circuit of succeeding stage. For this interstage coupling, different types of coupling elements can be employed.

They are

1. RC Coupling
2. Transformer Coupling.
3. Direct Coupling.

### RC Coupling:-

The circuit diagram RC coupled amplifier using transistor is shown below. The output signal of first stage is coupled to the input of the next stage through coupling capacitor and resistive load. at the output terminal of first stage.

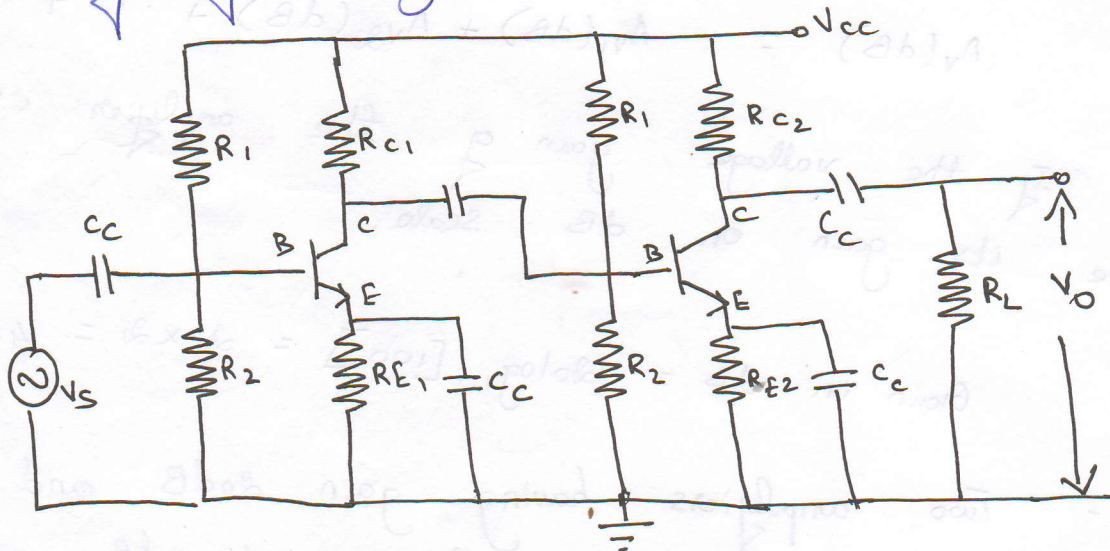


Fig. Two stage RC Coupled amplifier using transistor.

The coupling does not affect the quiescent point of the next stage. Since the coupling capacitor  $C_C$  blocks



This type of coupling is used to match the impedance between output and input cascaded stage. Usually it is used to match the large output resistance of AF power amplifiers to a low impedance load like loudspeakers.

The frequency response of a transformer coupled amplifier is poor on comparison with that of an RC coupled amplifier. Its leakage inductance and interwinding capacitance does not allow amplifier to amplify the signals of different frequencies equally well.

Interwinding capacitance of the transformer coupled may give rise resonance at certain frequency which makes amplifier to give very high gain at that frequency. By using shunting capacitors across each winding of the transformer we can get resonance at any desired RF frequency. Such an amplifier is called tuned voltage amplifier.



fig. Frequency response of transformer coupled amplifier.



the d.c voltage of the first stage from reaching the base of the second stage. The frequency response of RC Network drops off at very low frequencies due to coupling capacitors and also at high frequencies due to shunt capacitors such as stray capacitance.

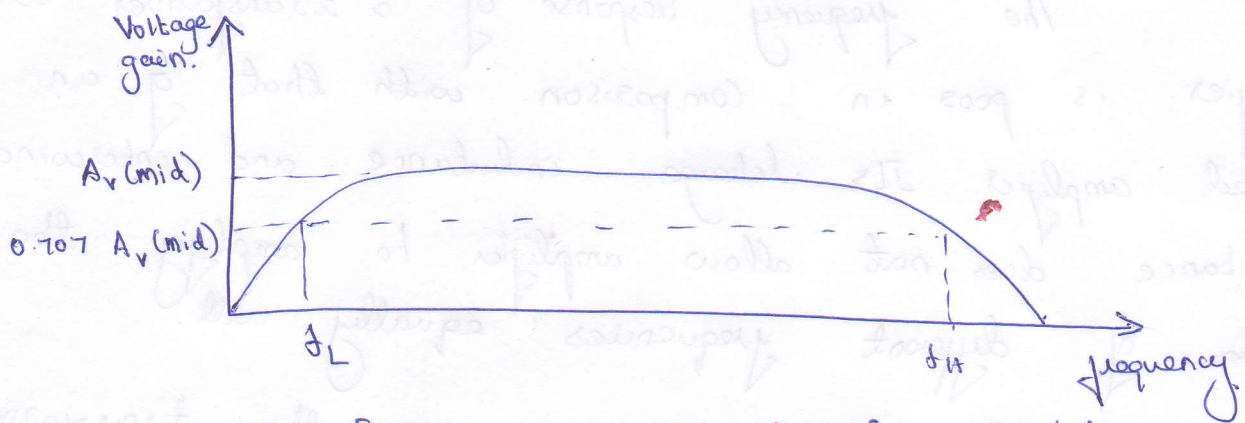
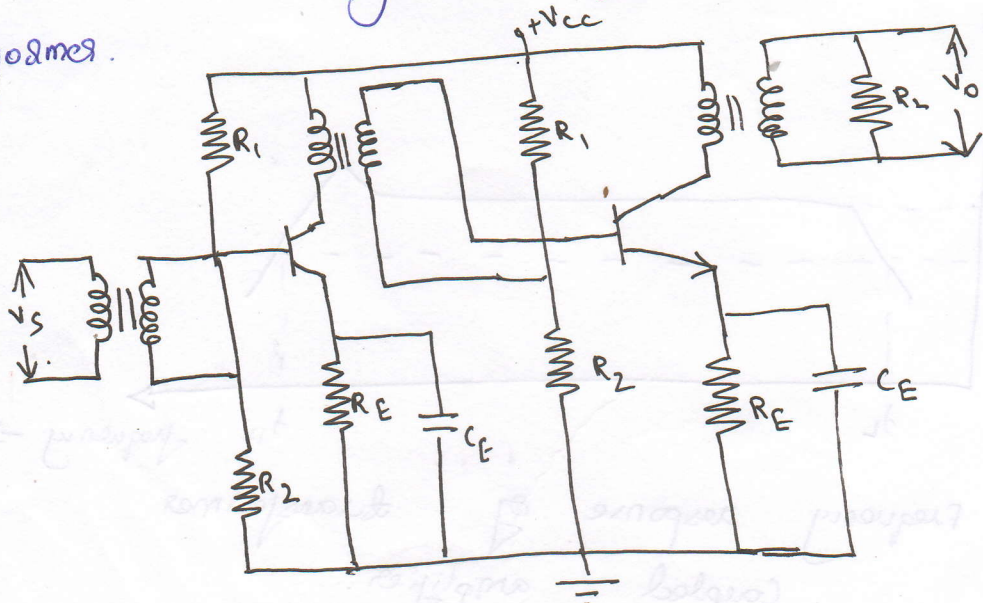


fig. Frequency response of RC Coupled Amplifier.

Transformer

Coupling: -

The circuit diagram for the transformer coupled amplifier using transistors is shown below. The output signal of first stage is coupled to the input of the next stage through an impedance matching transformer.



## Direct Coupling:-

The circuit diagram for direct coupled amplifier using transistor is shown below. The direct coupling allows the quiescent dc collector current of first stage to pass through base of the next stage, affecting its biasing condition.

Due to absence of RC components its low frequency is good but at higher frequencies shunting capacitors such as stray capacitances reduce the gain of the amplifier.

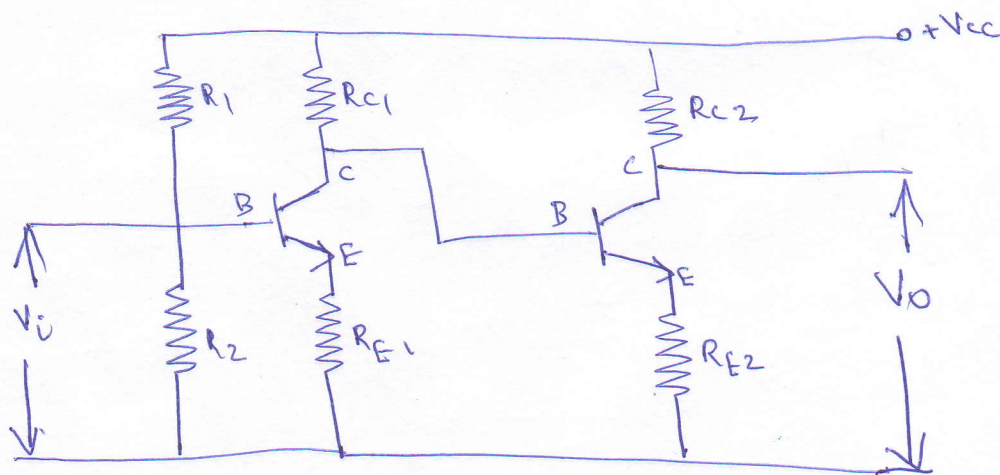


fig. Two stage direct coupled amplifier using transistor.

| Parameter           | RC Coupled             | Transformer Coupled            | Direct Coupled |
|---------------------|------------------------|--------------------------------|----------------|
| Coupling Components | Resistor and Capacitor | Impedance matching Transformer | -              |
| Block D.C           | Yes                    | Yes                            | No             |



|                     |                            |                                                                      |                                                                           |
|---------------------|----------------------------|----------------------------------------------------------------------|---------------------------------------------------------------------------|
| Frequency response. | Flat at middle frequencies | Not unipam, high at resonant frequency and low at other frequencies. | Flat at middle frequencies and improvement in the low frequency response. |
| Impedance matching  | Not achieved               | <del>Achieved</del><br>Achieved                                      | Not achieved                                                              |
| DC amplification    | No                         | No                                                                   | Yes                                                                       |
| Dist                | Not present                | Not present                                                          | Present.                                                                  |



Two stage amplifier with transformer coupling

|                     |                        |                   |
|---------------------|------------------------|-------------------|
| Transformer coupled | RC coupled             | Capacitor coupled |
| Impedance matching  | Resistor and capacitor | Capacitor         |
| DC                  | AC                     | DC                |

## Two stage RC coupled CE-CE Cascade Amplifier:-

The circuit diagram for the two stage CE-CE cascade amplifier with their biasing arrangement is shown below.

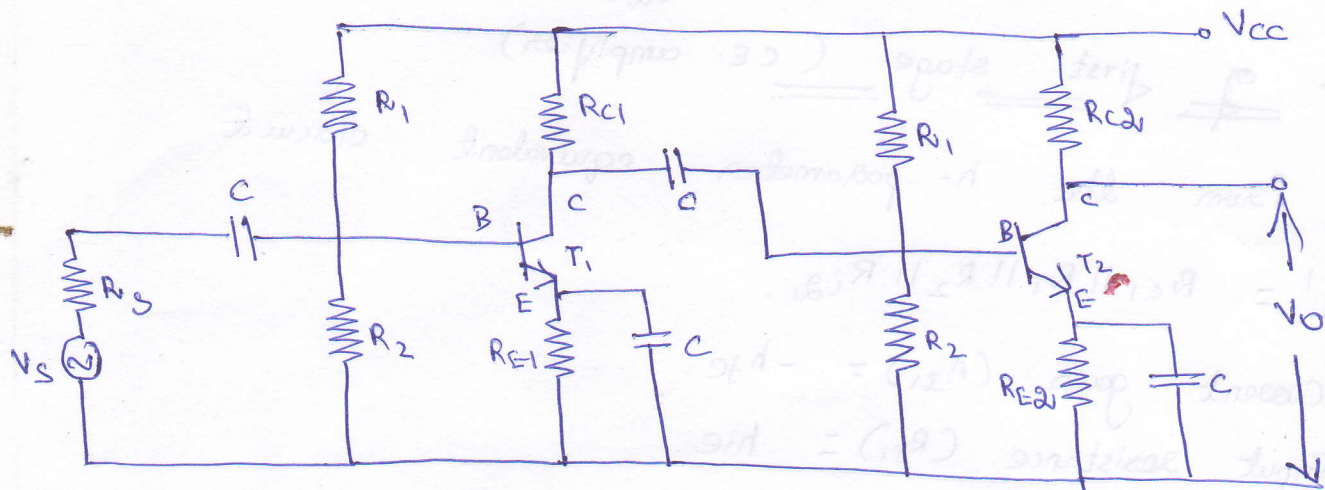


fig. CE-CE Cascade amplifier.

Let us assume all capacitors arbitrarily large and act as a short circuit for a.c. signal we can draw h-parameter equivalent circuit for CE-CE cascade amplifier as shown below.

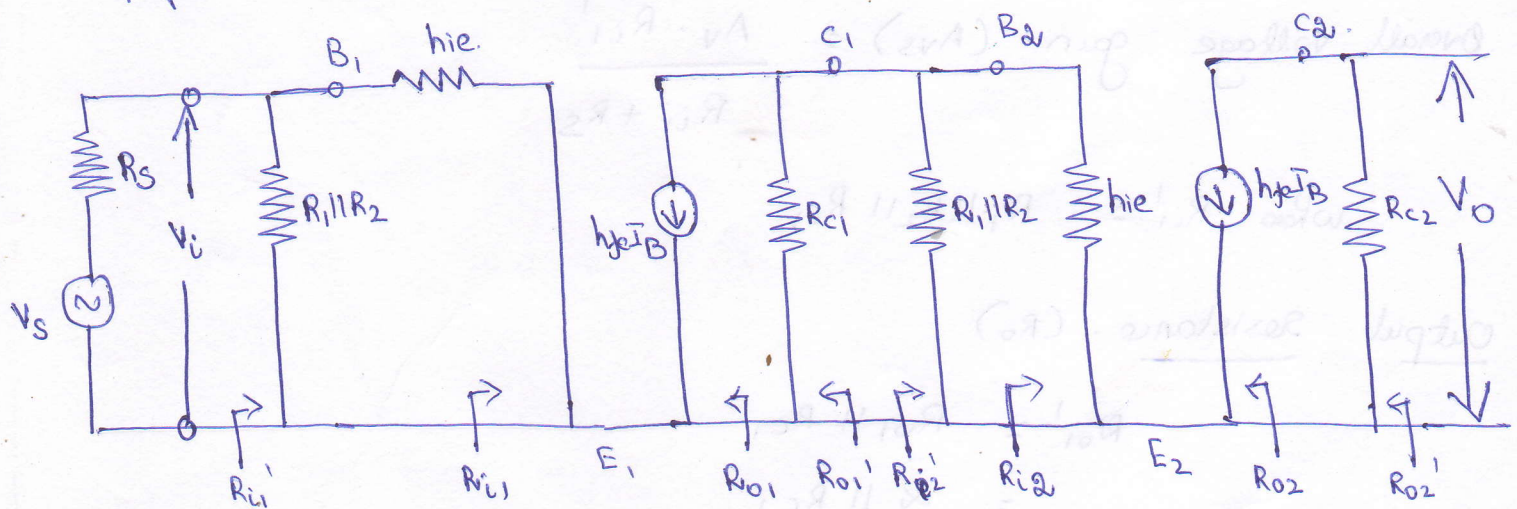


fig. Approximate h-parameter equivalent circuit for CE-CE cascade amplifier.



## Analysis of second stage (CE amplifier)

(a) Current gain ( $A_{I2}$ ) =  $-h_{fe}$

(b) Input resistance ( $R_{i2}$ ) =  $h_{ie}$ .

(c) Voltage gain ( $A_{v2}$ ) =  $\frac{A_{I2} \times R_L}{R_{i2}}$ .

## Analysis of first stage (CE amplifier)

From the h-parameter equivalent circuit

$$R_L' = R_{C1} \parallel R_1 \parallel R_2 \parallel R_{i2}.$$

a) Current gain ( $A_{I1}$ ) =  $-h_{fe}$ .

b) Input resistance ( $R_{i1}$ ) =  $h_{ie}$ .

c) Voltage gain ( $A_{v1}$ ) =  $\frac{A_{I1} \cdot R_L'}{R_{i1}}$

Voltage gain of cascade amplifier  $A_v = A_{v1} \cdot A_{v2}$

$$\therefore A_v = \left[ \frac{A_{I2} R_L}{R_{i2}} \right] \left[ \frac{A_{I1} R_L'}{R_{i1}} \right]$$

Overall voltage gain ( $A_{vs}$ ) =  $\frac{A_v \cdot R_{i1}'}{R_{i1}' + R_s}$

where  $R_{i1}' = R_1 \parallel R_2 \parallel R_{i1}$

## Output resistance ( $R_o$ )

$$R_{o1}' = R_{C1} \parallel R_{C1}$$

$$= \infty \parallel R_{C1}$$

$$= R_{C1}$$

$$R_{o2}' = R_{C2} \parallel R_{C2}$$

$$= \infty \parallel R_{C2}$$

$$= R_{C2}$$

//

## Two stage RC Coupled CE - CB Cascode Amplifier:-

The cascode amplifier consists of a common emitter stage in series with a common base amplifier stage as shown below. It is used to solve the low impedance problem of a common base circuit.

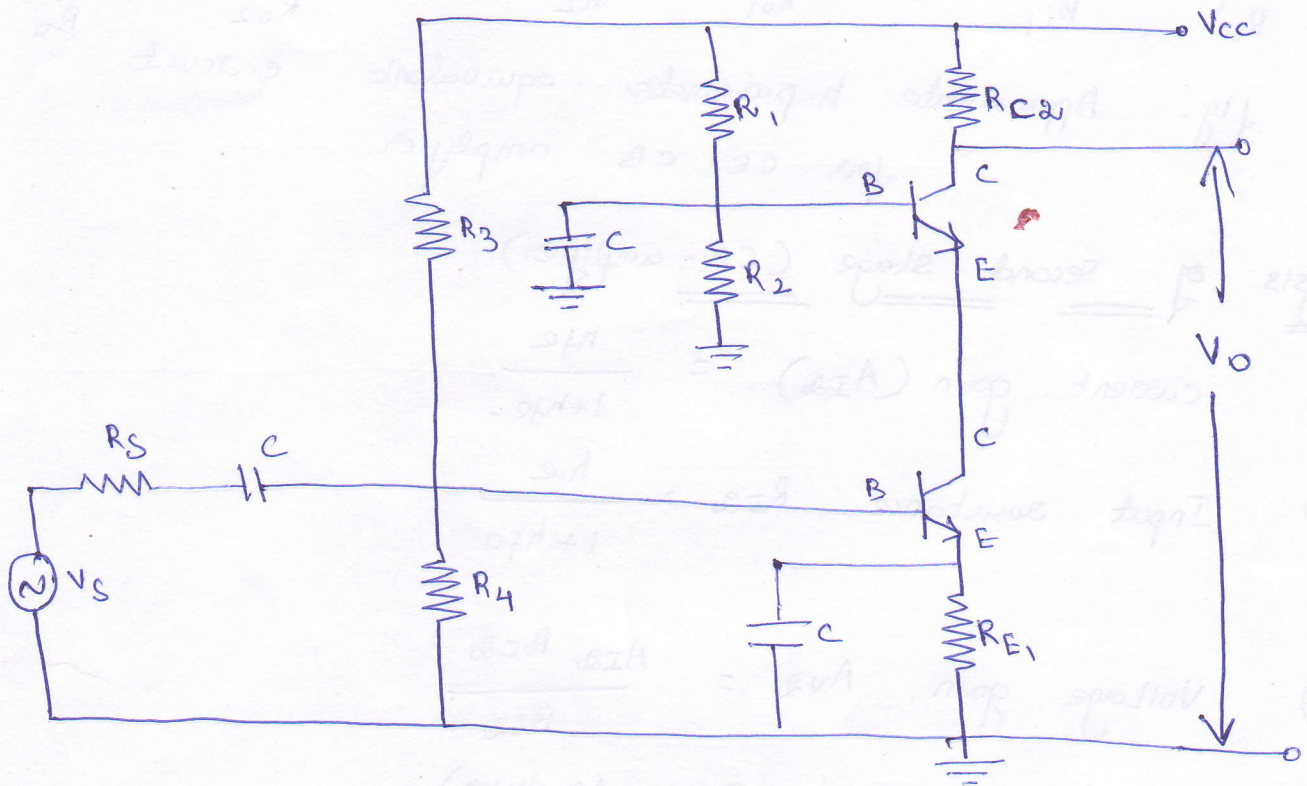


Fig. Cascode amplifier

### Feature:-

1. It provide high input impedance.
2. It provide high voltage gain.
3. It provide improved input-output isolation as there is no direct coupling from output to input.
4. It provide very high output resistance.
5. It also provides high slew rate and high stability.

The simplified h-parameter equivalent circuit for cascode amplifier is drawn by replacing transistors



with their simplified equivalent circuit as shown below.

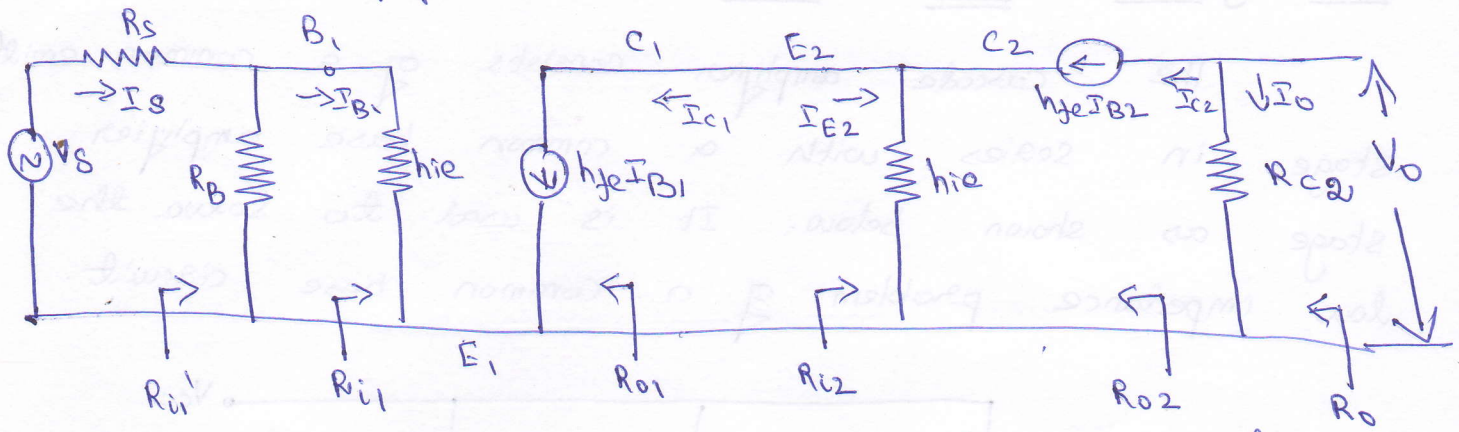


fig. Approximate h-parameter equivalent circuit for CE-CB amplifier.

Analysis of second stage (CB-amplifier)

(a) current gain  $(A_{I2}) = \frac{h_{fe}}{1+h_{fe}}$

(b) Input resistance  $R_{i2} = \frac{h_{ie}}{1+h_{fe}}$

(c) Voltage gain  $A_{v2} = \frac{A_{I2} R_{c2}}{R_{i2}}$

Analysis of first stage (CE-Amplifier)

(a) current gain  $(A_{I1}) = -h_{fe}$

(b) Input resistance  $(R_{i1}) = h_{ie}$

(c) Voltage gain  $(A_{v1}) = \frac{A_{I1} \cdot R_{c1}}{R_{i1}}$

Voltage gain of cascode amplifier  $(A_v) = A_{v1} \cdot A_{v2}$

$$A_v = \left[ \frac{A_{I2} \cdot R_{c2}}{R_{i2}} \right] \left[ \frac{A_{I1} \cdot R_{c1}}{R_{i1}} \right]$$

Overall input resistance  $R_{i1} = R_B \parallel R_{i1}$

$= R_3 \parallel R_4 \parallel R_{i1}$

Overall Voltage Gain ( $A_{Vs}$ ) :-

$$A_{Vs} = A_V \times \frac{R_{i1}}{R_{i1} + R_S}$$

Overall Current Gain ( $A_{Is}$ ) :-

$$A_{Is} = \frac{I_o}{I_s} = \frac{I_o}{I_{C2}} \times \frac{I_{C2}}{I_{E2}} \times \frac{I_{E2}}{I_{C1}} \times \frac{I_{C1}}{I_{B1}} \times \frac{I_{B1}}{I_s}$$

Where as,

$$\frac{I_o}{I_{C2}} = -1 ; \quad \frac{I_{C2}}{I_{E2}} = -A_{I2} ; \quad \frac{I_{E2}}{I_{C1}} = -1$$

$$\frac{I_{C1}}{I_{B1}} = -A_{I1} \quad \text{and} \quad \frac{I_{B1}}{I_s} = \frac{R_B}{R_B + R_{i1}}$$

$$\therefore A_{Is} = A_{I1} \cdot A_{I2} \left[ \frac{R_B}{R_B + R_{i1}} \right] //$$

Output Resistance :-

$$R_o = R_{o2} // R_{C2}$$

$$= \infty // R_{C2}$$

$$R_o = R_{C2} //$$

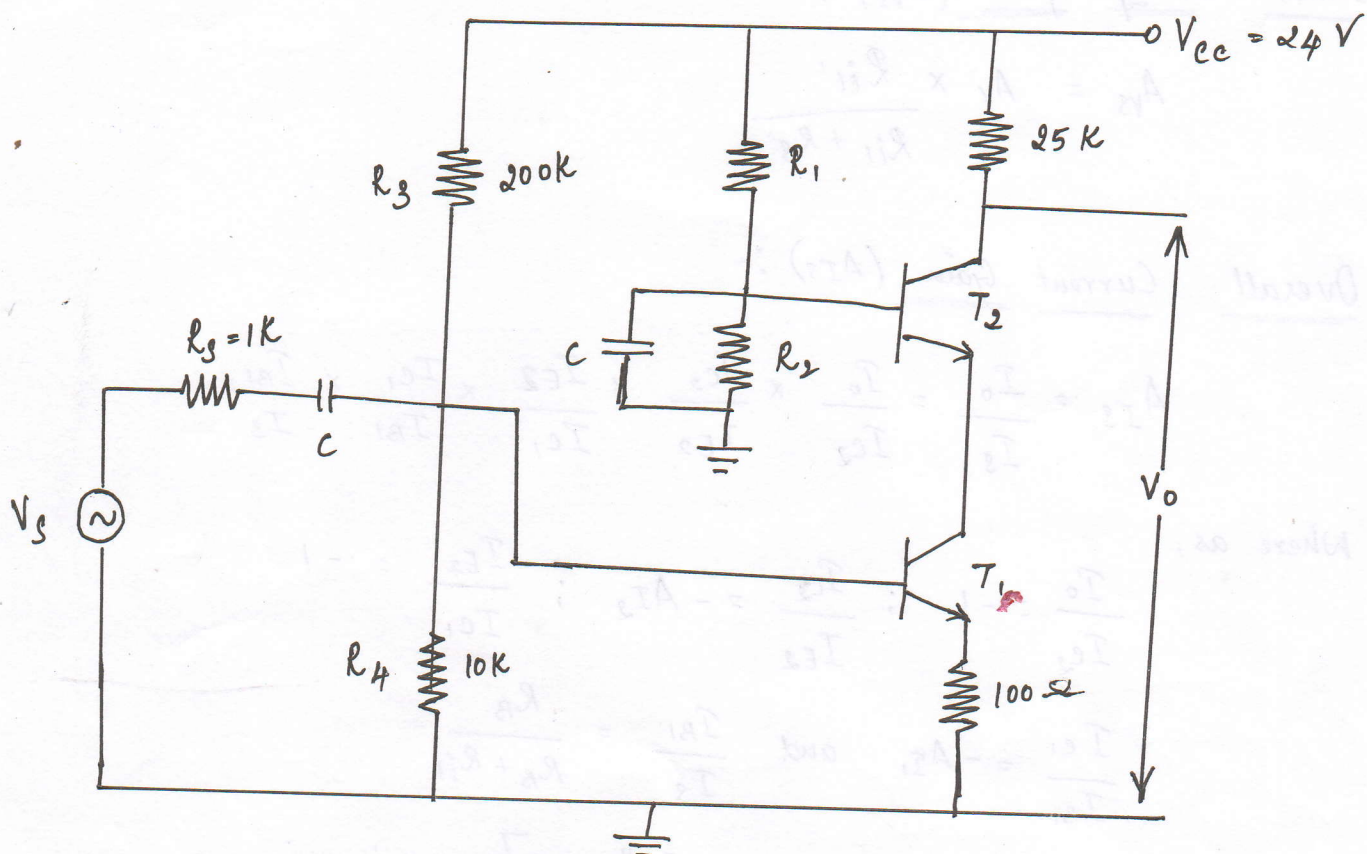
Disadvantage:

The only disadvantage of cascode circuit is that it requires two transistors and requires a relatively high supply voltage.

Problem: Calculate  $A_I$ ,  $A_V$ ,  $A_{Vs}$  and  $R_o$  for the Cascode circuit shown below, assume transistor are identical with

$$h_{fe} = 100, \quad h_{ie} = 2K\Omega \quad \text{and} \quad h_{re} = h_{ie} = 0$$





Analysis of Second Stage (CB amplifier):

- Current Gain ( $A_{i2}$ ) =  $\frac{h_{fe}}{1+h_{fe}} = \frac{50}{1+50} = 0.98$
- Input Resistance ( $R_{i2}$ ) =  $\frac{h_{ie}}{1+h_{fe}} = \frac{1.1K}{1+50} = 21.56 \Omega$
- Voltage Gain ( $A_{v2}$ ) =  $\frac{A_{i2} R_{L2}}{R_{i2}} = \frac{0.98 \times 3K}{21.56} = 136.36$

Analysis of first stage (CE amplifier):

- Current Gain ( $A_{i1}$ ) =  $-h_{fe} = -50$
- Input Resistance ( $R_{i1}$ ) =  $h_{ie} = 1.1K$
- Voltage Gain ( $A_{v1}$ ) =  $\frac{A_{i1} R_{i2}}{R_{i1}}$

$$= \frac{-50 \times 21.56}{1.1K} = -0.98$$

$$\text{Voltage Gain of Cascode amplifier } A_v = A_{v1} \times A_{v2} = -0.98 \times 136.36 = -133.63$$

Overall input resistance ( $R_{ci}$ ) =  $R_{ci} \parallel R_B = R_{ci} \parallel R_3 \parallel R_4$

$$R_{ci} = 200k \parallel 10k \parallel 12.1k$$

$$R_{ci} = 5.328 k\Omega$$

Overall Voltage gain ( $A_{vs}$ ):

$$A_v = A_v \times \frac{R_{ci}}{R_{ci} + R_s} = -204.5 \times \frac{5.32k}{5.32k + 1k}$$

$$A_v = -172.18 //$$

Overall Current gain ( $A_I$ )

$$A_I = A_{I1} \cdot A_{I2} \left[ \frac{R_B}{R_B + R_{ci}} \right]$$

$$= (0.99) \times (100) \times \left[ \frac{9.52 \times 10^3}{9.52 \times 10^3 + 12.1k} \right]$$

$$A_I = -43.6 //$$

Output resistance ( $R_o$ )

$$R_o = R_{o2} \parallel R_{c2}$$

$$= 6 \parallel 25k$$

$$R_o = 25k$$

BiCMOS AMPLIFIER:

The bipolar junction transistors have a large transconductance than MOS transistors biased at the same current level and they have higher switching speed. Due to large transconductance they provide large voltage gain.



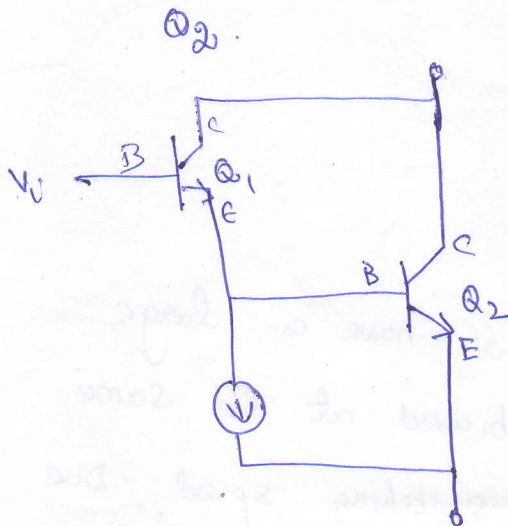
MOS transistors have an essentially infinite input impedance at low frequencies and have very high packaging density. Due to almost infinite input impedance, MOS transistors have zero input bias circuit current.

The advantages of these two technologies can be exploited by combining bipolar and MOS transistors on the same integrated circuit. Such technology is called BiCMOS Technology.

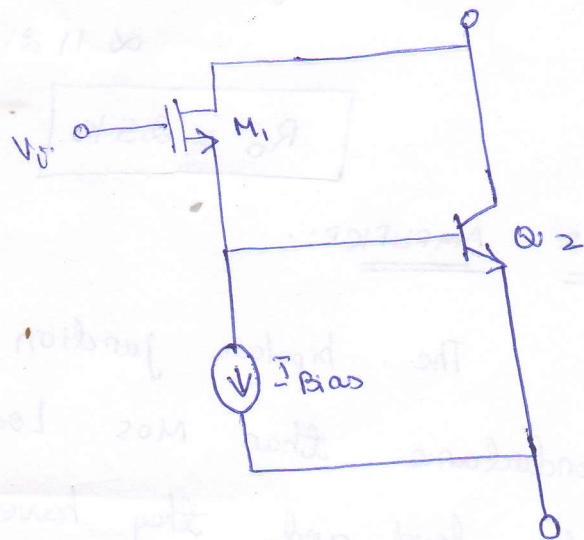
### Basic Amplifier stages:-

The circuit diagram for the Darlington pair and BiCMOS Darlington pair is shown below. In BiCMOS Darlington pair the transistor  $Q_1$  is replaced by a MOSFET. This circuit has following advantages.

- (i) An infinite input resistance.
- (ii) A large transconductance due to bipolar transistor



(a) Bipolar Darlington pair configuration.



(b) BiCMOS Darlington pair configuration.

Analysis:

The small signal equivalent circuit of BiCMOS darlington pair is shown below let us assume  $r_o = \infty$  in both the transistors.

From the small signal equivalent circuit output current can be written as

$$I_o = g_{m1}V_{gs} + g_{m2}V_{\pi} \quad \text{--- (1)}$$

and input voltage can be written as

$$V_o = V_{gs} + V_{\pi} \quad \text{--- (2)}$$

and

$$V_{\pi} = g_{m1}V_{gs}r_{\pi} \quad \text{--- (3)}$$

Now substitute eqn (3) in (2)

$$V_o = V_{gs} + g_{m1}V_{gs}r_{\pi}$$

$$= V_{gs} [1 + g_{m1}r_{\pi}]$$

$$\therefore V_{gs} = \frac{V_i}{[1 + g_{m1}r_{\pi}]} \quad \text{--- (4)}$$

Substitute eqn (3) in (1) we get.

$$I_o = g_{m1}V_{gs} + g_{m2}g_{m1}V_{gs}r_{\pi}$$

$$I_o = g_{m1}V_{gs} [1 + g_{m2}r_{\pi}] \quad \text{--- (5)}$$

Now substitute eqn (4) in (5) we get.

$$I_o = \frac{g_{m1} [1 + g_{m2}r_{\pi}] V_i}{[1 + g_{m1}r_{\pi}]} \quad \text{--- (6)}$$

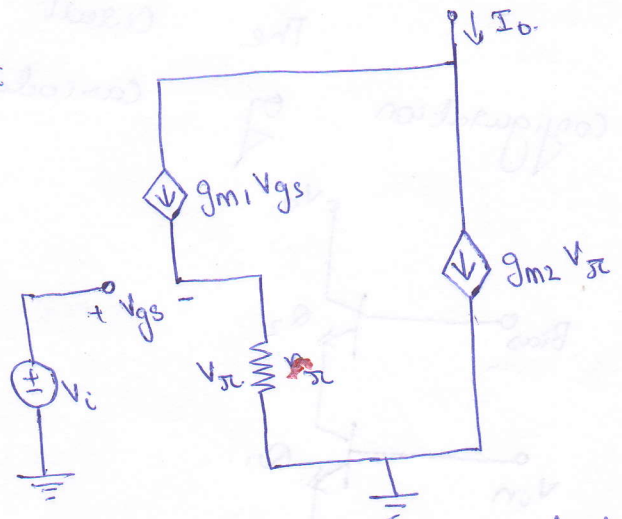


Fig. Small signal equivalent circuit of BiCMOS Darlington.

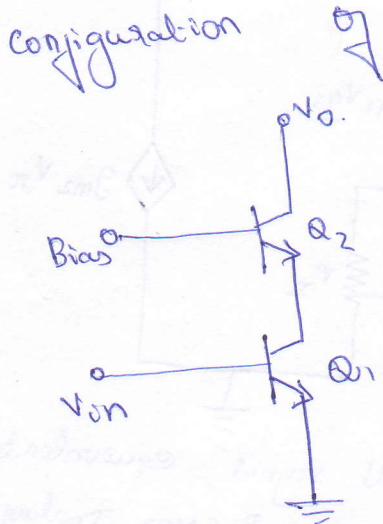
we get.



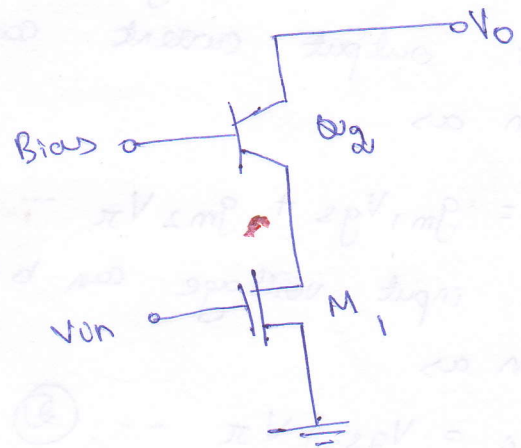
where  $I_0 = g_m^c V_0$   $\therefore g_m^c = \frac{g_{m1}(1 + g_{m2}r_{\pi})}{(1 + g_{m1}r_{\pi})}$   
 and  $g_m^c$  is Composite transconductance.

### Cascode Amplifier:

The circuit diagram and BICMOS cascode configuration is shown below.



(a) Bipolar Cascode Configuration.



(b) BICMOS Cascode Configuration

### Differential Amplifier:

The differential amplifier amplifies the difference between two input voltage signal.  
 Let  $V_1$  and  $V_2$  are the two input signals  
 in an ideal differential amplifier, the output voltage  $V_0$  is proportional to the difference between the two input signal.

$$V_0 \propto [V_1 - V_2]$$

### Differential Gain ( $A_d$ ):

$$V_o = A_d (V_1 - V_2)$$

where  $A_d$  is the proportionality constant. Hence it is called differential gain of the differential amplifier.

The difference between the two input ( $V_1 - V_2$ ) is called difference voltage denoted as  $V_d$ .

$$\therefore V_o = A_d V_d$$

Hence differential gain can be expressed as

$$A_d = \frac{V_o}{V_d}$$

Generally differential gain is expressed in decibel (dB)

$$A_d = 20 \log_{10} (A_d) \text{ in dB.}$$

### Common mode Gain ( $A_c$ ):

Practically differential amplifier not only depend on the difference voltage but also depends on the average common level of the two inputs. This is called common mode ~~gain~~ signal denoted as  $A_c V_c$ .

$$V_c = \frac{V_1 + V_2}{2}$$

The gain with which it amplifies the common mode signal to produce the output is called common mode gain.

$$V_o = A_c V_c$$



So the total output of any differential amplifier can be expressed as

$$V_o = A_d V_d + A_c V_c$$

Common Mode Rejection Ratio :- (CMRR)

The ability of a differential amplifier to reject a common mode signal is expressed by a ratio called common mode rejection ratio denoted as CMRR.

It is also defined as the ratio of differential voltage gain  $A_d$  to common mode voltage gain  $A_c$

$$CMRR = \left| \frac{A_d}{A_c} \right|$$

CMRR in terms of dB is

$$CMRR = 20 \log_{10} \left| \frac{A_d}{A_c} \right| \text{ dB} //$$

Features of Differential Amplifier:-

1. High differential voltage gain
2. low common mode gain
3. high input impedance
4. large Bandwidth.
5. low offset voltages and current.
6. low output impedance.

## Differential Mode Operation:

In the differential mode, the two input signals are different from each other. i.e. it has same magnitude but  $180^\circ$  out of phase. These signals with opposite phase can be obtained from the center tap transformer.

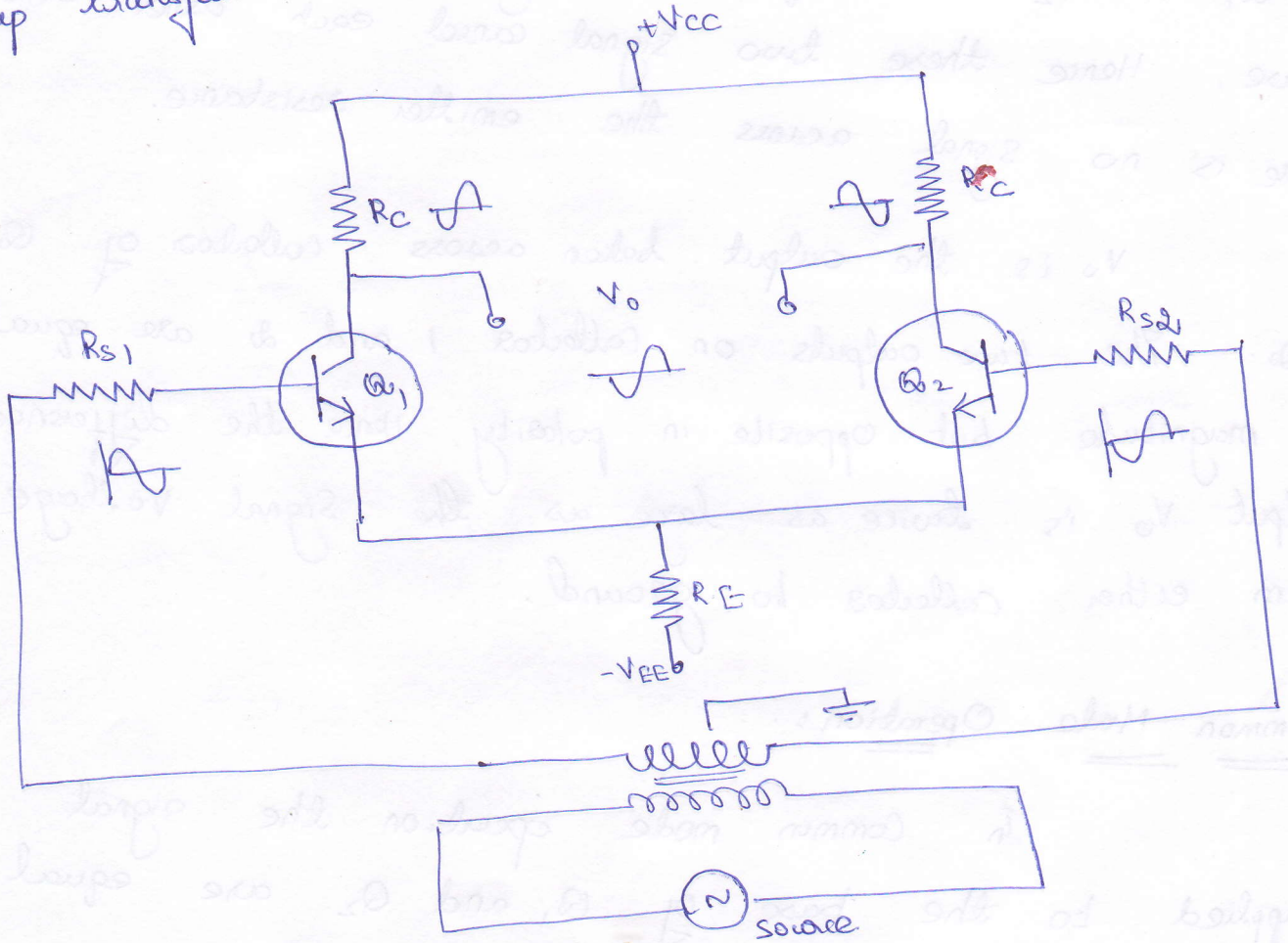


Fig. Differential Mode

With a positive going signal on the base of  $Q_1$ , an amplified negative going signal develops on the collector of  $Q_1$ . Due to positive going signal current through  $R_E$  also increases and hence a positive going wave is developed across  $R_E$ .



Due to negative going signal on the base of  $Q_2$ , an amplified positive going signal develops on the collector of  $Q_2$  and a negative going signal develops across  $R_E$ .

So signal voltage across  $R_E$  due to the effect of  $Q_1$  and  $Q_2$  are equal in magnitude and  $180^\circ$  out of phase. Hence these two signals cancel each other and there is no signal across the emitter resistance.

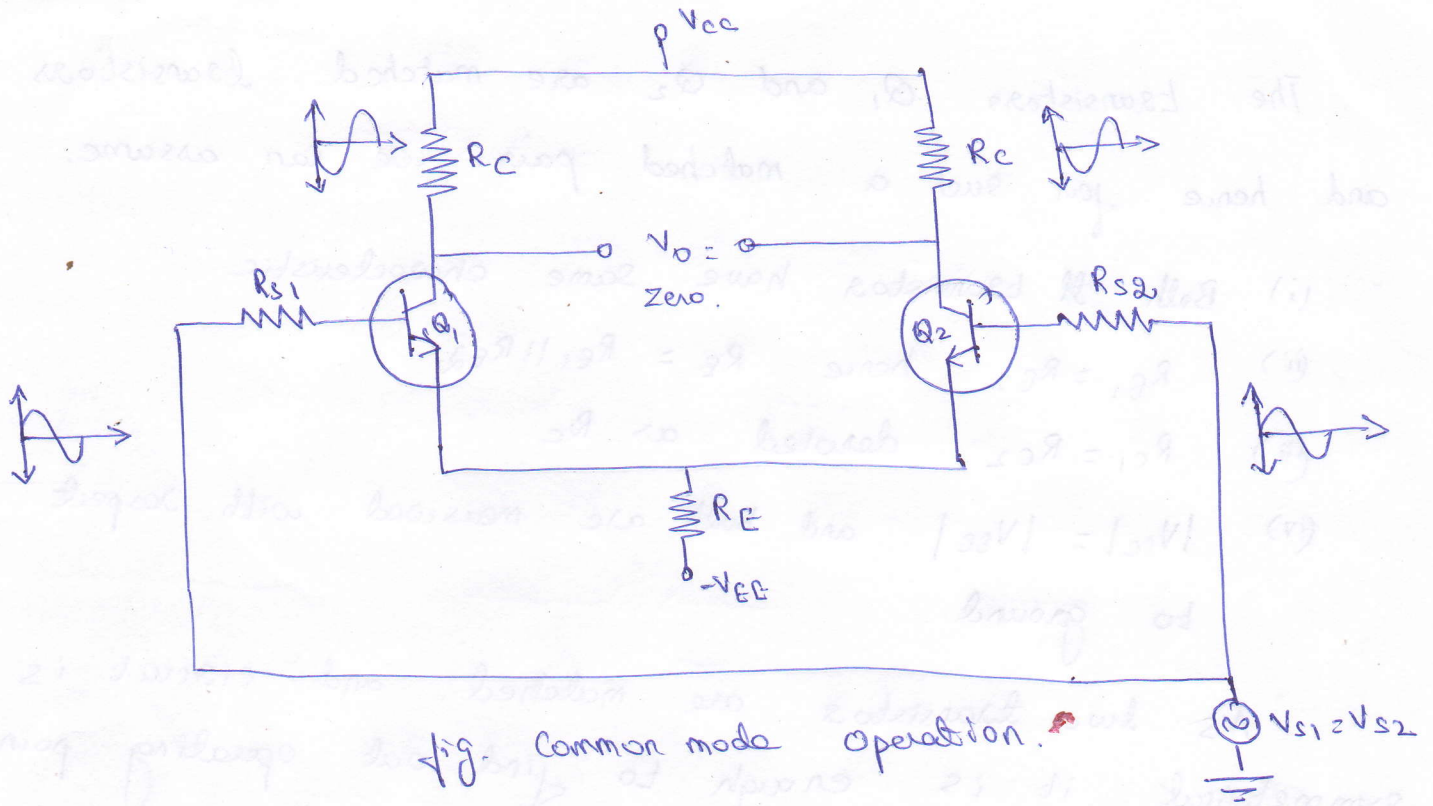
$V_o$  is the output taken across collector of  $Q_1$  and  $Q_2$ . The two outputs on collector 1 and 2 are equal in magnitude but opposite in polarity. Hence the difference output  $V_o$  is twice as large as the signal voltage from either collector to ground.

### Common Mode Operation:

In common mode operation the signal applied to the base of  $Q_1$  and  $Q_2$  are equal in magnitude as well as in phase.

In phase signal voltages at the bases of  $Q_1$  and  $Q_2$  causes in phase signal voltage to appear across  $R_E$ , which added together.

Hence  $R_E$  carries a signal current and provides a negative feedback. This feedback reduces the common mode gain of differential amplifier.



### DC Analysis of Differential Amplifier:

The dc analysis means to obtain the operating point value  $I_{CQ}$  and  $V_{CEQ}$  for the transistor used. The supply voltage are dc while the input signals are ac. So dc equivalent circuit can be obtained simply by reducing the input ac signals to zero. The d-c equivalent circuit is shown below.

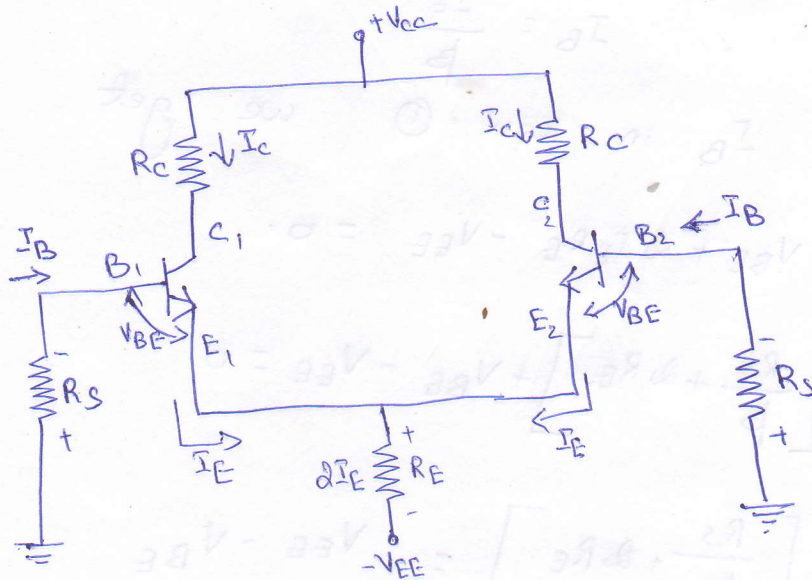


fig. DC equivalent circuit



The transistors  $Q_1$  and  $Q_2$  are matched transistors and hence for such a matched pair we can assume.

- (i) Both ~~the~~ transistors have same characteristic
- (ii)  $R_{E1} = R_{E2}$  hence  $R_E = R_{E1} \parallel R_{E2}$
- (iii)  $R_{C1} = R_{C2}$  denoted as  $R_C$
- (iv)  $|V_{CC}| = |V_{EE}|$  and both are measured with respect to ground.

As two transistors are matched and circuit is symmetrical it is enough to find out operating point  $I_{CQ}$  and  $V_{CEQ}$  for any one of the two transistors. The same is applicable for other transistor.

Apply KVL to Base-emitter loop of transistor  $Q_1$

$$I_B R_S + V_{BE} + 2I_E R_E - V_{EE} = 0 \quad \dots \textcircled{1}$$

we know that  $I_C = \beta I_B \Rightarrow I_B = \frac{I_C}{\beta}$

where  $I_C \approx I_E$

$$\therefore I_B = \frac{I_E}{\beta}$$

Now substitute  $I_B$  in equ  $\textcircled{1}$  we get

$$\frac{I_E R_S}{\beta} + V_{BE} + 2I_E R_E - V_{EE} = 0$$

$$I_E \left[ \frac{R_S}{\beta} + 2R_E \right] + V_{BE} - V_{EE} = 0$$

$$I_E \left[ \frac{R_S}{\beta} + 2R_E \right] = V_{EE} - V_{BE}$$

$$I_E = \frac{V_{EE} - V_{BE}}{\left[ \frac{R_S}{\beta} + 2R_E \right]} \quad \text{--- (2)}$$

Practically  $\frac{R_S}{\beta} \ll 2R_E$

$$\therefore I_E = \frac{V_{EE} - V_{BE}}{2R_E} \quad \text{--- (3)}$$

$$[I_E = I_C]$$

Apply KVL to the transistor @ output terminal we get.

$$V_C = V_{CC} - I_C R_C \quad \text{--- (4)}$$

Neglecting the drop across  $R_S$ . Hence collector to emitter voltage is

$$V_{CE} = V_C - V_E$$

$$[V_E = -V_{BE}]$$

$$= [V_{CC} - I_C R_C] - (-V_{BE}) \quad \text{--- (5)}$$

$$V_{CE} = V_{CC} - I_C R_C + V_{BE} \quad \text{--- (6)}$$

## AC analysis of differential amplifiers

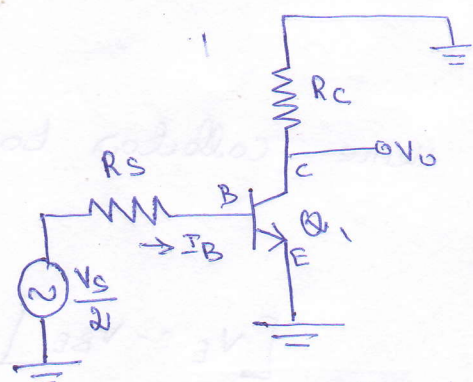
In the ac analysis we will calculate the differential gain  $A_d$ , common mode gain  $A_c$ , input resistance  $R_i$  and the output resistance  $R_o$  of the differential amplifier using h-parameter.

### Differential Gain ( $A_d$ ):

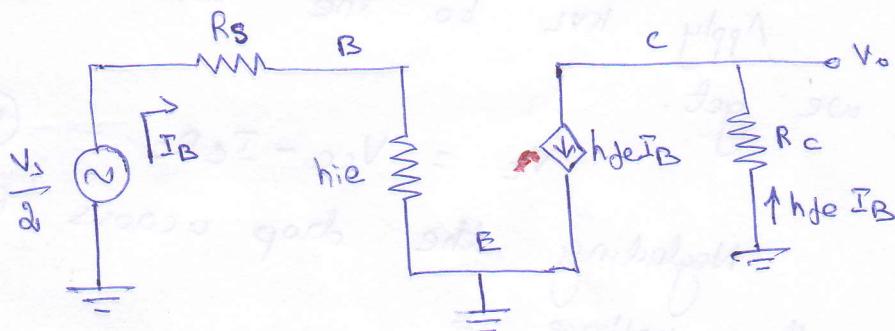
For the differential gain calculation, the two ac input signals are equal in magnitude but having  $180^\circ$  phase difference in between them.



The magnitude of each a.c input voltage  $V_{s1}$  and  $V_{s2}$  be  $V_s/2$ . The two a.c. emitter currents  $I_{e1}$  and  $I_{e2}$  are equal in magnitude and  $180^\circ$  out of phase. Hence they cancel each other to get resultant a.c current through the emitter as zero. Hence for the a.c purpose emitter terminal can be grounded.



(a) AC equivalent circuit



(b) Approximate hybrid model.

The approximate hybrid model for the above circuit can be shown above.

Apply KVL to the input loop we get

$$\frac{V_s}{2} = I_B R_s + I_B h_{ie} \quad \text{--- (1)}$$

$$= I_B [R_s + h_{ie}]$$

$$\therefore I_B = \frac{V_s}{2 [R_s + h_{ie}]} \quad \text{--- (2)}$$

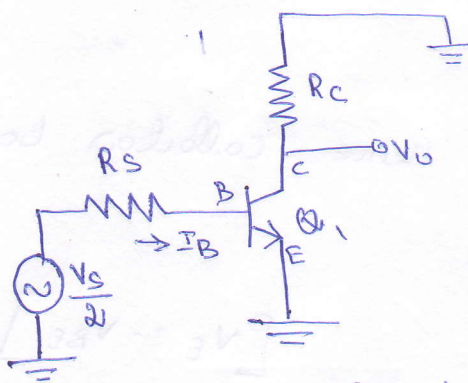
Apply KVL to the output loop we get.

$$V_o = -h_{fe} I_B R_c \quad \text{--- (3)}$$

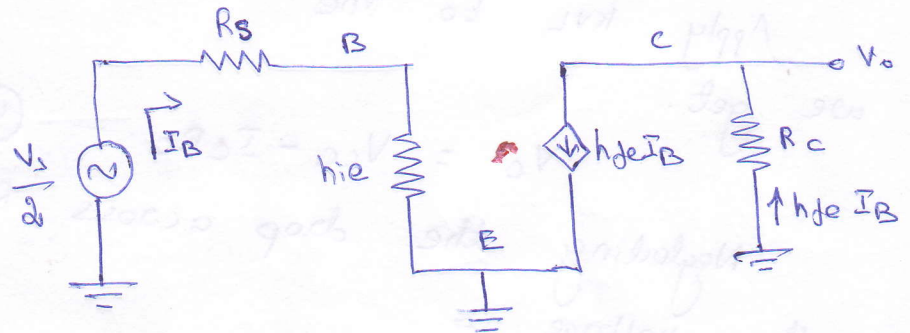
Substitute eqn (2) in (3) we get.

$$V_o = -h_{fe} \left[ \frac{V_s}{2 (R_s + h_{ie})} \right] R_c \quad \text{--- (3)}$$

The magnitude of each a.c input voltage  $V_{s1}$  and  $V_{s2}$  be  $V_s/2$ . The two a.c. emitter currents  $I_{e1}$  and  $I_{e2}$  are equal in magnitude and  $180^\circ$  out of phase. Hence they cancel each other to get resultant a.c current through the emitter as zero. Hence for the a.c purpose emitter terminal can be grounded.



(a) AC equivalent circuit



(b) Approximate hybrid model.

The approximate hybrid model for the above circuit can be shown above.

Apply KVL to the input loop we get

$$\frac{V_s}{2} = I_B R_s + I_B h_{ie} \quad \text{--- (1)}$$

$$= I_B [R_s + h_{ie}]$$

$$\therefore I_B = \frac{V_s}{2 [R_s + h_{ie}]} \quad \text{--- (2)}$$

Apply KVL to the output loop we get.

$$V_o = -h_{fe} I_B R_c \quad \text{--- (3)}$$

Substitute eqn (2) in (3) we get.

$$V_o = -h_{fe} \left[ \frac{V_s}{2 (R_s + h_{ie})} \right] R_c \quad \text{--- (3)}$$



$$\frac{V_o}{V_s} = \frac{-h_{fe} R_c}{2[R_s + h_{ie}]} \quad \text{--- (4)}$$

The applied two input signal magnitude are  $\frac{V_s}{2}$  but they are opposite in polarity as  $180^\circ$  out of phase.

$$V_d = V_1 - V_2 = \frac{V_s}{2} - \left(-\frac{V_s}{2}\right) = V_s$$

replace  $V_s$  by  $V_d$  in equ (4) we get.

$$A_d = \frac{V_o}{V_d} = \frac{-h_{fe} R_c}{2(R_s + h_{ie})} \quad \text{(for unbalanced output)} \quad \text{--- (5)}$$

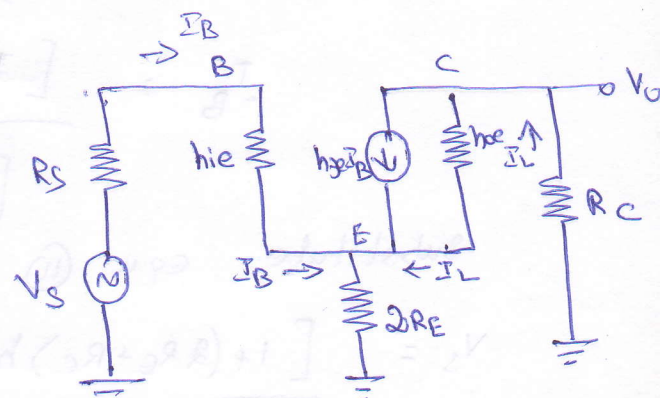
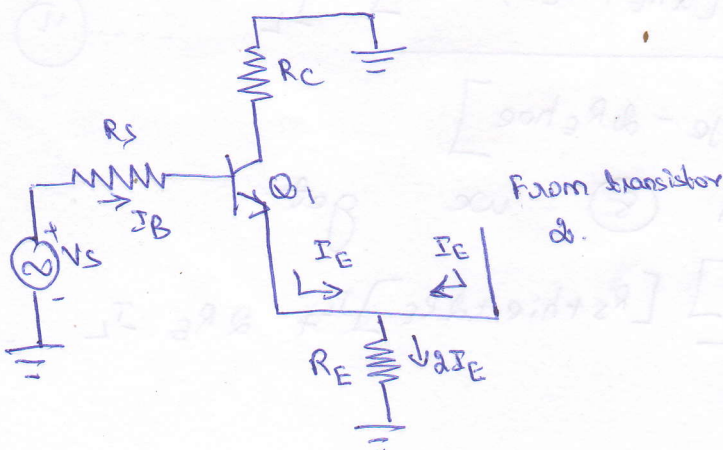
Hence the expression for  $A_d$  with balanced output as

$$A_d = 2 \cdot \left[ \frac{-h_{fe} R_c}{2(R_s + h_{ie})} \right]$$

$$A_d = \frac{-h_{fe} R_c}{R_s + h_{ie}} \quad \text{(Balanced Output)} \quad \text{--- (6)}$$

### Common Mode Gain ( $A_c$ ):

In common mode gain the magnitude of both the ac input signal be  $V_s$  and are in phase with each other. therefore both the emitter current  $I_{E1} = I_{E2} = I_E$  flow through  $R_E$  in the same direction.



Approximate hybrid model.

Hence the total current flow through  $R_E$  is  $2I_E$ .  
The approximate hybrid model for the above circuit is shown above.

Apply KVL to the input we get.

$$V_S = I_B R_S + I_B h_{ie} + 2R_E (I_B + I_L) \quad \text{--- (7)}$$

$$V_S = I_B [R_S + h_{ie} + 2R_E] + 2R_E I_L \quad \text{--- (8)}$$

and Output voltage  $V_O$  is written as

$$V_O = -I_L R_C \quad \text{--- (9)}$$

Now apply KVL to the output loop we get

$$\frac{(I_L - h_{fe} I_B)}{h_{oe}} + 2R_E (I_L + I_B) + I_L R_C = 0 \quad \text{--- (10)}$$

$$\frac{I_L}{h_{oe}} - \frac{h_{fe} I_B}{h_{oe}} + 2R_E I_L + 2R_E I_B + I_L R_C = 0$$

$$I_L \left[ \frac{1}{h_{oe}} + 2R_E + R_C \right] - I_B \left[ \frac{h_{fe}}{h_{oe}} - 2R_E \right] = 0$$

$$I_L \left[ \frac{1}{h_{oe}} + 2R_E + R_C \right] = I_B \left[ \frac{h_{fe}}{h_{oe}} - 2R_E \right]$$

$$\frac{I_L}{h_{oe}} \left[ \frac{1 + (2R_E + R_C) h_{oe}}{h_{oe}} \right] = I_B \left[ \frac{h_{fe} - 2R_E h_{oe}}{h_{oe}} \right]$$

$$I_B = \frac{[1 + (2R_E + R_C) h_{oe}]}{[h_{fe} - 2R_E h_{oe}]} I_L \quad \text{--- (11)}$$

Substitute equ (11) in (8) we get.

$$V_S = \frac{[1 + (2R_E + R_C) h_{oe}]}{[h_{fe} - 2R_E h_{oe}]} [R_S + h_{ie} + 2R_E] I_L + 2R_E I_L \quad \text{--- (12)}$$



$$\frac{V_s}{I_L} = \frac{[1 + 2R_E h_{oe} + R_c h_{oe}][R_s + h_{ie} + 2R_E] + 2R_E [h_{je} - 2R_E h_{oe}]}{[h_{je} - 2R_E h_{oe}]}$$

$$\left\{ \begin{aligned} &R_s + h_{ie} + 2R_E + 2R_E h_{oe} R_s + 2R_E h_{oe} h_{ie} + 4R_E h_{oe} + \\ &R_c R_s h_{oe} + R_c h_{oe} h_{ie} + 2R_E R_c h_{oe} + 2R_E h_{je} - 4R_E h_{oe} \end{aligned} \right\}$$

$$\frac{V_s}{I_L} = \frac{[h_{je} - 2R_E h_{oe}]}{[h_{je} - 2R_E h_{oe}]} \cdot \frac{2R_E [1 + h_{je}] + R_s [1 + 2R_E h_{oe}] + h_{ie} [1 + 2R_E h_{oe}] + h_{oe} R_c [R_s + h_{ie} + 2R_E]}{[h_{je} - 2R_E h_{oe}]} \quad \dots (13)$$

Neglecting the terms of  $h_{oe} R_c$  because practically  $h_{oe} R_c \ll 1$   
 Therefore equation (13) become.

$$\frac{V_s}{I_L} = \frac{2R_E (1 + h_{je}) + R_s (1 + 2R_E h_{oe}) + h_{ie} (1 + 2R_E h_{oe})}{[h_{je} - 2R_E h_{oe}]}$$

$$\frac{V_s}{I_L} = \frac{2R_E (1 + h_{je}) + (R_s + h_{ie}) (1 + 2R_E h_{oe})}{[h_{je} - 2R_E h_{oe}]} \quad \dots (14)$$

From the above expression rearrange and find

$$I_L = \frac{(h_{je} - 2R_E h_{oe}) V_s}{2R_E (1 + h_{je}) + (R_s + h_{ie}) (1 + 2R_E h_{oe})}$$

Substitute  $I_L$  in equ (9) we get.

$$V_o = \frac{(h_{je} - 2R_E h_{oe}) V_s R_c}{2R_E (1 + h_{je}) + (R_s + h_{ie}) (1 + 2R_E h_{oe})}$$

$$\frac{V_o}{V_s} = \frac{(2R_E h_{fe} - h_{fe}) R_c}{2R_E(1+h_{fe}) + (R_s + h_{ie})(1+2R_E h_{fe})} \quad \text{--- (15)}$$

For common mode, input  $V_c$  is the average value of two.

$$\therefore V_c = \frac{V_1 + V_2}{2} = \frac{V_s + V_s}{2} = \frac{2V_s}{2} = V_s$$

$\therefore$  Replace  $V_s$  by  $V_c$  and neglect  $h_{fe}$  parameter in equ (15) we get

$$A_c = \frac{V_o}{V_c} = \frac{-h_{fe} R_c}{2R_E(1+h_{fe}) + (R_s + h_{ie})} \quad \text{--- (16)}$$

The expression for CMRR is obtained as

$$CMRR = \left| \frac{A_d}{A_c} \right| = \left| \frac{\frac{+h_{fe} R_c}{R_s + h_{ie}}}{\frac{-h_{fe} R_c}{2R_E(1+h_{fe}) + R_s + h_{ie}}} \right|$$

$$CMRR = \frac{R_s + h_{ie} + 2R_E(1+h_{fe})}{R_s + h_{ie}} \quad \text{--- (17)}$$

Differential input impedance:

From equ (2) the input impedance of differential amplifier can be written as

$$R_i = \frac{V_s}{I_B} = 2(R_s + h_{ie}) \quad \text{--- (18)}$$



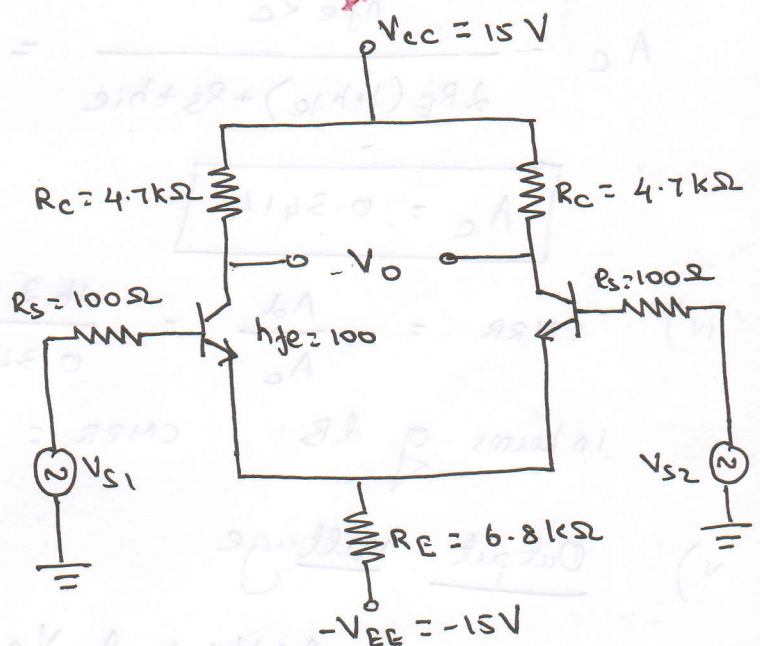
## Output impedance ( $R_o$ )

It is defined as the equivalent resistance between one of the output terminals with respect to ground.

$$R_o = R_c$$

Problem: The below fig shows dual input balanced output differential amplifier configuration. Assuming Silicon transistor with  $h_{ie} = 2.8 k\Omega$  Calculate.

- (i) Operating point values
- (ii) Differential gain
- (iii) Common mode gain
- (iv) CMRR
- (v) Output if  $V_{s1} = 70 mV$  peak to peak at  $1 kHz$  and  $V_{s2} = 40 mV$  peak to peak at  $1 kHz$



Solution:-

- (i) Operating point  $I_{CQ}$  and  $V_{CEQ}$  to be find.

$$I_{CQ} = I_E = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_S}{\beta}}$$

where  $\beta = h_{FE} = 100$

assume  $V_{BE} = 0.7 V$

$$= \frac{15V - 0.7}{2(6.8 \times 10^3) + \frac{100}{100}}$$

$I_{CQ} = 1.05 mA$



$$V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$$

$$= 15 + 0.7 - [1.05 \times 10^{-3} \times 4.7 \times 10^3]$$

$$V_{CEQ} = 10.758 \text{ V}$$

ii) Differential mode gain:-

$$A_d = \frac{h_{fe} R_C}{R_s + h_{ie}} = \frac{100 \times 4.7 \times 10^3}{100 + 2.8 \times 10^3} = 162.068$$

iii) Common mode gain:-

$$A_c = \frac{h_{fe} R_C}{2R_E(1+h_{fe}) + R_s + h_{ie}} = \frac{100 \times 4.7 \times 10^3}{2 \times 6.8 \times 10^3 (1+100) + 100 + 2.8 \times 10^3}$$

$$A_c = 0.3414$$

$$\text{iv) } CMRR = \frac{A_d}{A_c} = \frac{162.68}{0.34} = 474.65$$

in terms of dB

$$CMRR = 20 \log_{10}(474.65) = 53.527 \text{ dB}$$

v) Output voltage

$$V_o = A_d V_d + A_c V_c$$

$$V_d = V_{s1} - V_{s2} = 70\text{m} - 40 = 30\text{mV}$$

$$V_c = \frac{V_{s1} + V_{s2}}{2} = \frac{70 \times 10^{-3} + 40 \times 10^{-3}}{2} = 55\text{mV}$$

$$\therefore V_o = (162.07)(30 \times 10^{-3}) + (0.34)(55 \times 10^{-3})$$

$$V_o = 4.862 + 0.018$$

$$V_o = 4.88 \text{ V}$$

$$A_{m20.1} = 0.5$$

## Single Tuned Amplifier:-

To amplify the selective range of frequencies the resistive load,  $R_c$  is replaced by a tuned circuit. The tuned circuit is capable of amplifying a signal over a narrow band of frequencies centered at  $f_r$ . An amplifier with such a tuned circuit as a load are known as tuned amplifier.

Since tuned amplifier amplify narrow band of ~~narrow~~ frequencies they are also known as narrow band amplifiers.

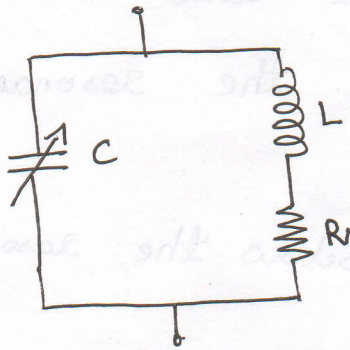


Fig. Tuned Circuit

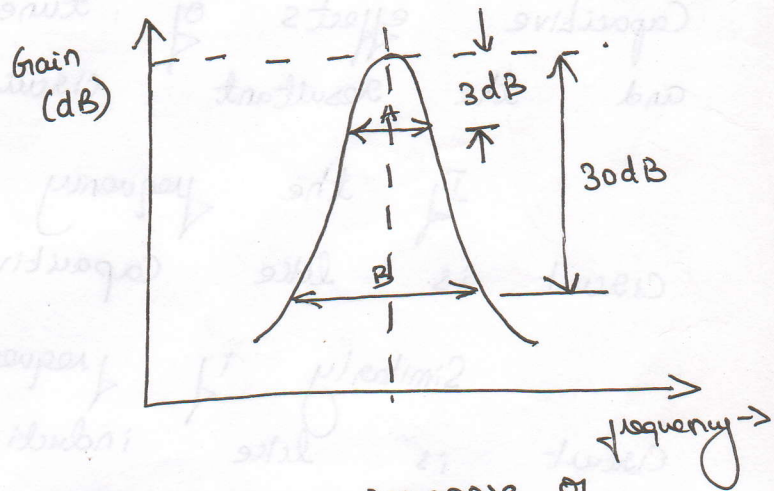


Fig. Frequency response of Tuned amplifier.

The above figure shows the tuned parallel LC circuit which resonates at a particular frequency. The resonance frequency and impedance of tuned circuit is given as

$$\text{Resonance frequency. } (f_r) = \frac{1}{2\pi\sqrt{LC}} \quad \dots (1)$$

$$\text{Impedance } (Z_r) = \frac{L}{CR} \quad \dots (2)$$



The response of tuned amplifiers is maximum at resonant frequency and it falls sharply for frequencies below and above the resonant frequency. Thus the tuned amplifier designed to reject all frequencies below and above the lower and upper cut off frequency.

As shown in frequency response curve the ratio of 30 dB bandwidth (B) to 3 dB bandwidth (A) is known as skirt selectivity.

At resonance frequency, the inductive and capacitive effects of tuned circuit cancel each other and the resultant circuit is like resistive.

If the frequency above the resonance frequency, circuit is like capacitive.

Similarly if frequency below the resonance frequency, circuit is like inductive.

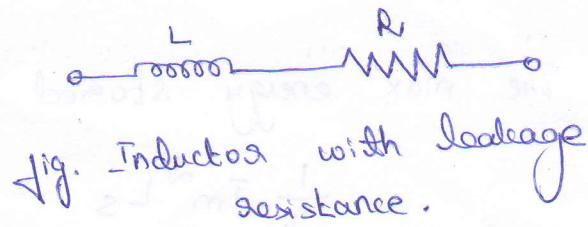
### Coil losses:-

The tuned circuit consists of inductive coil. practically, the coil is not purely inductive. It consists of few losses and they are represented in the form of leakage resistance in series with the inductor. Refer circuit diagram of tuned amplifiers.

The total loss in the coil is comprised of



- (i) Copper loss
- (ii) eddy current loss
- (iii) hysteresis loss.



Quality factor :- [ Q - Factor ]

The Q-factor is the ratio of reactance to resistance and therefore it is unitless.

The Q-factor can also be defined as the measure of efficiency with which inductor can store the energy.

$$Q = 2\pi \cdot \frac{\text{Maximum energy stored per cycle}}{\text{Energy dissipated per cycle.}} \quad (2)$$

Dissipation factor (D) :-

It can be referred as the total loss with in a component and it is simply defined as

$$D = \frac{1}{Q}$$

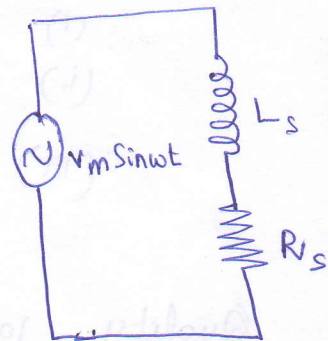
Expression for quality factor of an inductor :-

Consider the circuit shown below, here the sinusoidal voltage  $V_m \sin \omega t$  is applied to the inductor with an internal resistor  $R_s$ .

The max energy stored per cycle is  $\left[ \frac{I_m}{\sqrt{2}} \right]^2 R_s$

$$\frac{1}{2} I_m^2 L_s \quad \dots \textcircled{1}$$

Average power dissipated per cycle =  $\left[ \frac{I_m}{\sqrt{2}} \right]^2 R_s \quad \dots \textcircled{2}$



w.k.t Energy = Power  $\times$  Time.

fig. Circuit for obtain equation (2).

$\therefore$  Average energy dissipated per cycle

$$= \text{Power} \times \text{Periodic time for one cycle.} \quad \dots \textcircled{3}$$

Now substitute (2) in (3) we get

$$= \left[ \frac{I_m^2}{2} \right] \frac{R_s}{f}$$

$$\left[ T = \frac{1}{f} \right]$$

$$\therefore \text{Average energy dissipated per cycle} = \frac{I_m^2 R_s}{2f} \quad \dots \textcircled{4}$$

we know that expression for quality factor.

$$Q = 2\pi \frac{\text{Max Energy stored per cycle}}{\text{Energy dissipated per cycle}} \quad \dots \textcircled{5}$$

Substitute eqn (1) & (4) in (5) we get

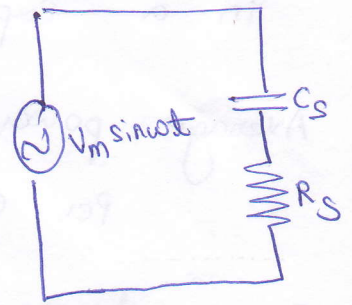
$$Q = 2\pi \frac{\frac{1}{2} I_m^2 L_s}{\frac{I_m^2 R_s}{2f}} = \frac{2\pi f L_s}{R_s}$$

$$Q = \frac{\omega L_s}{R_s} \quad \dots \textcircled{6}$$



## Expression for quality factor of a Capacitor:-

Consider the circuit shown in fig. where sinusoidal voltage  $V_m \sin \omega t$  is applied to the Capacitor with a small resistor.



Max energy stored in the capacitor per cycle  $= \frac{1}{2} C_s V_{\max}^2$  --- (1)

Circuit for obtain equation of Q.

where  $V_{\max} = \frac{I_m}{\omega C_s}$  when  $R_s \ll \frac{1}{\omega C_s}$

Substitute  $V_{\max}$  in equ (1) we get

Max energy stored in the capacitor per cycle  $= \frac{1}{2} C_s \cdot \left[ \frac{I_m^2}{\omega^2 C_s^2} \right] = \frac{I_m^2}{2 \omega^2 C_s}$  (2)

Energy dissipated per cycle  $= \frac{I_m^2 R_s}{2 f}$  --- (3)

Now substitute equ (2) & (3) in quality factor

$Q = 2\pi \cdot \frac{\text{Max Energy stored per Cycle}}{\text{Energy dissipated per cycle.}}$

$= 2\pi \cdot \frac{\frac{I_m^2}{2 \omega^2 C_s}}{\frac{I_m^2 R_s}{2 f}} = \frac{1}{\omega C_s R_s} //$

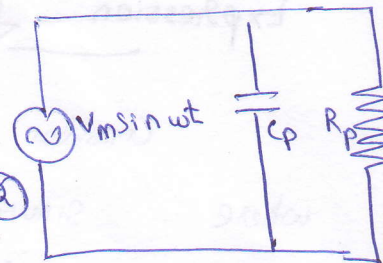
## Capacitor with high resistor in parallel:-

Consider a circuit shown below, where a sinusoidal voltage  $V_m \sin \omega t$  is applied to the Capacitor with high resistor in parallel.



Maximum energy stored in a capacitor  $= \frac{1}{2} C_p V_{\max}^2$  --- (1)

Average power dissipated per cycle  $= \left( \frac{V_{\max}}{\sqrt{2}} \right)^2 \times \frac{1}{R_p} = \frac{V_{\max}^2}{2 R_p}$  --- (2)



Circuit for obtain equation of Q.

Energy dissipated per cycle  $= \frac{V_{\max}^2}{2 R_p} \times T$   
 $= \frac{V_{\max}^2}{2 R_p f}$  --- (3)

Now substitute equ (1) & (3) in quality factor

$$Q = 2\pi \frac{\frac{1}{2} C_p V_{\max}^2}{\frac{V_{\max}^2}{2 R_p f}} = 2\pi f R_p C_p.$$

$$Q = \omega R_p C_p. \quad \text{--- (4)}$$

Unloaded and loaded Q :-

when the tank circuit is not connected to any external circuit or load, Q account for the internal losses and it is known as unloaded quality factor  $Q_u$ .

$$Q_u = 2\pi \frac{\text{Maximum energy stored per cycle}}{\text{Energy dissipated per cycle in tank circuit.}}$$

Practically, the tank circuit is connected to the load. Hence, the energy dissipation



takes place in the tank circuit as well as in the external load. The loaded quality factor is

$$Q_L = 2\pi \times \frac{\text{(Maximum energy stored per cycle)}}{\left[ \begin{array}{l} \text{Energy dissipated per cycle in tank circuit} + \\ \text{Energy dissipated per cycle due to presence} \\ \text{of external load.} \end{array} \right]}$$

Then the equivalent parallel resistance  $R_p$  is reduced by any external resistance  $R_{ext}$  placed in parallel with the circuit.

$$\therefore Q_L = \frac{R_T}{\omega L P} \quad \text{where } R_T = R_p \parallel R_{ext}$$

The quality factor  $Q_L$  determine the 3 dB bandwidth for the resonant circuit. The 3dB bandwidth for resonant circuit is given as

$$BW = \frac{f_r}{Q_L}$$

Problem:- A tuned Amplifier has its maximum gain at a frequency of 2 MHz and has a bandwidth of 50 kHz. Calculate the Q factor.

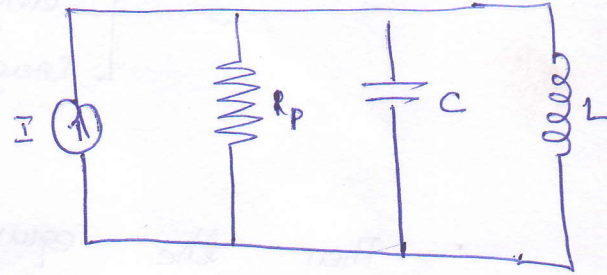
Given:-  $f_r = 2 \text{ MHz}$  and  $BW = 50 \text{ kHz}$ .

$$\therefore Q = \frac{f_r}{BW} = \frac{2 \times 10^6}{50 \times 10^3} = 40 //$$

## Parallel resonant Circuit :-

The circuit diagram for the tuned parallel LC circuit which resonates at a particular frequency is shown below.

The total admittance of the parallel tuned circuit can be written as



Parallel resonant LC Circuit

$$Y_T = \frac{1}{R_p} + \frac{1}{1/j\omega C} + \frac{1}{j\omega L} \quad \text{--- (1)}$$

$$= \frac{1}{R_p} + j\omega C + \frac{1}{j\omega L}$$

$$= \frac{1}{R_p} + j \left[ \omega C - \frac{1}{\omega L} \right] \quad \text{--- (2)}$$

At resonance frequency imaginary part is zero  
∴ from equation (2)

$$\omega C - \frac{1}{\omega L} = 0$$

$$\omega C = \frac{1}{\omega L}$$

$$[\omega = 2\pi f]$$

$$f = \frac{1}{2\pi \sqrt{LC}} \quad \text{--- (3)}$$

The quality factor expression for the parallel inductor circuit is

$$Q = \frac{R_p}{\omega L} \quad \text{--- (4)}$$



Similarly for capacitor circuit

$$Q = \omega C R_p \quad \dots (5)$$

Compare equ (4) & (5) we get.

$$\omega C R_p = \frac{R_p}{\omega L}$$

$$\omega^2 C L = 1 \quad \dots (6)$$

At resonance frequency reactance equal to zero  
therefore from equ (6).

$$Y_T = \frac{1}{R_p} \quad \dots (7)$$

$\therefore$  Impedance at resonance  $Z_0 = R_p \quad \dots (8)$

Substitute  $R_p$  in equ (4) & (5) we get-

$$Q = \frac{Z_0}{\omega L} \Rightarrow Z_0 = Q \omega L \quad \dots (9)$$

and.  $Q = \omega C Z_0 \Rightarrow Z_0 = \frac{Q}{\omega C} \quad \dots (10)$

Compare equ (9) & (10) we get.

$$Z_0 = Q \omega L = \frac{Q}{\omega C} \quad \dots (11)$$

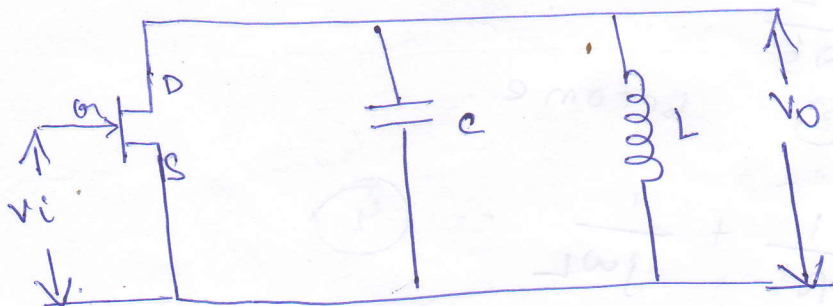


Fig. LC resonant circuit.

$$\therefore A_v = -g_m R_L$$

$$A_v = -g_m R_{o \parallel L}$$

Series Resonant Circuit :-

The circuit diagram for series resonant circuit is shown below. Here the loss element  $R_s$  is in series with  $L$ .

The admittance of the  $R_s L$  series branch is

$$Y = \frac{1}{R_s + j\omega L} \quad \text{--- (1)}$$

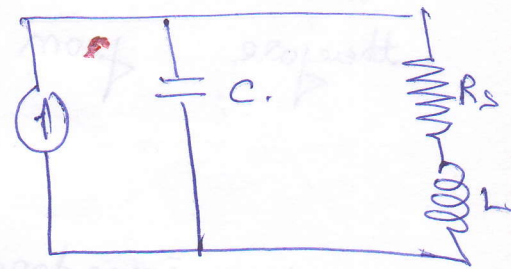


Fig.  $R_s$  in Series

multiply (num) and denominator by  $(R_s - j\omega L)$  we get.

$$Y = \frac{R_s - j\omega L}{(R_s^2 + \omega^2 L^2)} \quad \text{--- (2)}$$

$$Y = \frac{R_s}{\omega^2 L^2} + \frac{1}{j\omega L} \quad \left[ R_s^2 \ll \omega^2 L^2 \text{ so we can neglect } \right] \quad \text{--- (3)}$$

assign.  $R' = \frac{\omega^2 L^2}{R_s}$

eqn (3) become.

$$Y = \frac{1}{R'} + \frac{1}{j\omega L} \quad \text{--- (4)}$$

we know that for parallel circuit quality factor can be written as.

$$Q = \omega C R_p \quad \text{--- (5)}$$

replace  $R_p$  by  $R_s$  in equ (5) we get.

$$Q = \omega C R_s = \omega C \frac{\omega^2 L^2}{R_s} \quad \text{--- (6)}$$

wkt  $\omega^2 LC = 1$

$$\therefore Q = \frac{\omega L}{R_s}$$

Problem: A resonant circuit has  $C = 120 \text{ pF}$ ,  $L = 100 \mu\text{H}$  (with a series resistance of  $5 \text{ ohms}$ ). Find the quality factor and bandwidth of the circuit.

Given that :-  $C = 120 \text{ pF}$ ;  $L = 100 \mu\text{H}$ ,  $R_s = 5 \Omega$

Sol:-

$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{100 \times 10^{-6} \cdot 120 \times 10^{-12}}} = 1.45 \text{ MHz}$$

$$\omega = 2\pi f = 2 \times 3.14 \times 1.45 \text{ MHz} = 9.128 \times 10^6$$

$$Q = \frac{\omega L}{R_s} = \frac{9.13 \times 10^6 \times 100 \times 10^{-6}}{5} = 182.57$$

$$BW = \frac{f_r}{Q} = \frac{1.45 \times 10^6}{182.57} = 7.957 \text{ kHz}$$



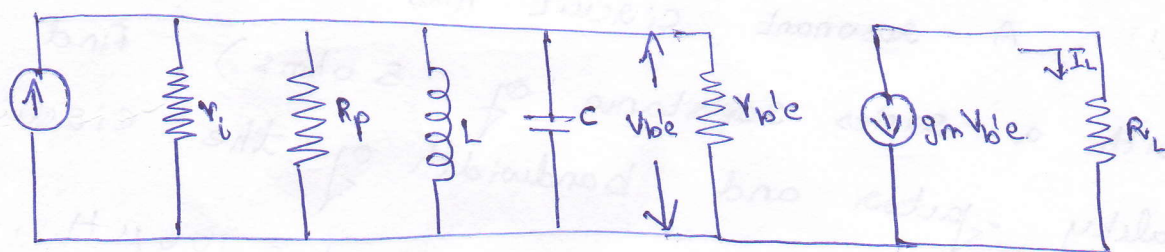
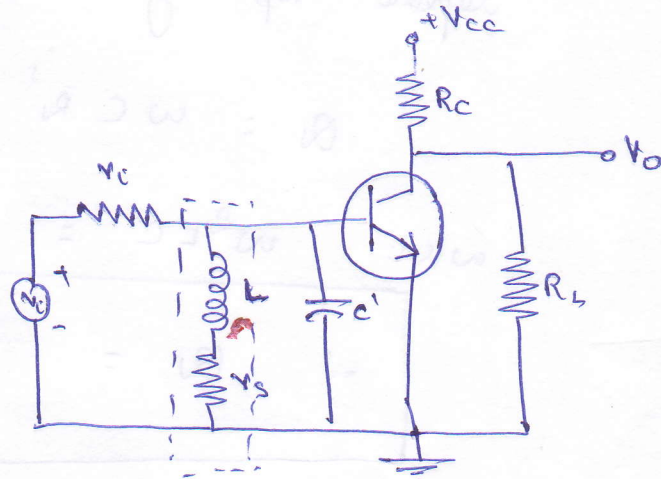
# Single Signal Tuned Transistor Amplifier

A Common emitter amplifier can be converted into a single tuned amplifier by including a parallel tuned circuit as shown below.

Assume.

$$R_L \ll R_C \text{ and } r_{bb'} = 0$$

The simplified equivalent circuit for a single tuned amplifier using hybrid  $\pi$  model is shown below.



The series  $R_L$  circuit is replaced by a equivalent  $R_L$  circuit in above fig. assuming coil losses are low over the frequency band of interest

$$\therefore \text{w.r.t } Q = \frac{\omega L}{r_s} \gg 1 \quad \text{--- (1)}$$

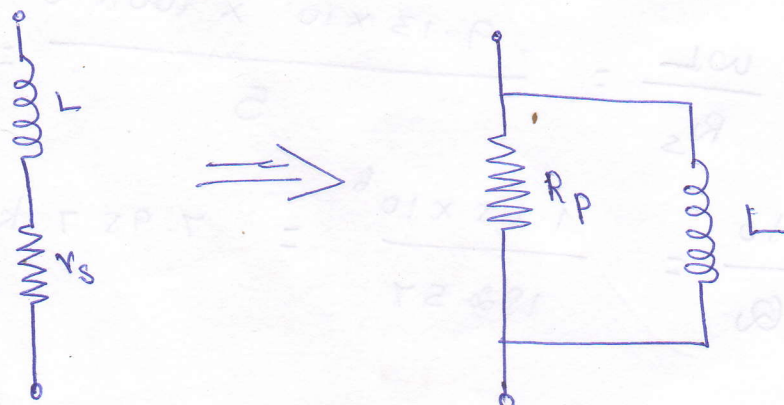


Fig. Equivalent circuit.

The admittance equation for the above equivalent circuit can be written as

$$Y = \frac{1}{r_s + j\omega L} \quad \text{--- (2)}$$

multiply num and denominator by  $r_s - j\omega L$  we get

$$Y = \frac{r_s - j\omega L}{r_s^2 + \omega^2 L^2}$$

$$Y = \frac{r_s}{r_s^2 + \omega^2 L^2} - \frac{j\omega L}{r_s^2 + \omega^2 L^2} \quad \text{--- (3)}$$

where as  $\omega L \gg r_s$  therefore above equation become

$$Y = \frac{r_s}{\omega^2 L^2} + \frac{1}{j\omega L} \quad \text{--- (4)}$$

$$Y = \frac{1}{R_p} + \frac{1}{j\omega L} \quad \text{--- (5)}$$

where  $\frac{1}{R_p} = \frac{r_s}{\omega^2 L^2} = \frac{r_s \times r_s}{\omega^2 L^2 \cdot r_s} = \frac{r_s^2}{r_s \omega^2 L^2} \quad \text{--- (6)}$

we know that  $Q_c = \frac{\omega L}{r_s}$  [for series parallel inductor]

$$\therefore r_s Q_c = \omega L$$

replace  $\omega L$  by  $r_s Q_c$  in the above equation (6)

$$\frac{1}{R_p} = \frac{r_s^2}{r_s \cdot r_s Q_c^2} = \frac{1}{r_s Q_c^2}$$

$$\therefore R_p = r_s Q_c^2 \quad \text{--- (7)}$$



Consider the small signal equivalent circuit.

$$R = r_i \parallel R_p \parallel r_{b'e} \quad \dots (8)$$

The current gain of the amplifier is then

$$A_I = \frac{-g_m R}{1 + j(\omega R C - R/\omega L)}$$

$$= \frac{-g_m R}{1 + j\omega_0 R C [\omega/\omega_0 - \omega_0/\omega]} \quad \dots (9) \quad \omega_0^2 = \frac{1}{LC}$$

The quality factor  $Q$  of the tuned circuit at resonant frequency  $\omega_0$  be.

$$Q = \frac{R}{\omega_0 L} = \omega_0 R C \quad \dots (10)$$

$\therefore$  equ (9) become,

$$A_I = \frac{-g_m R}{1 + jQ[\omega/\omega_0 - \omega_0/\omega]} \quad \dots (11)$$

when  $\omega = \omega_0$  condition for max gain

$$A_I(\max) = -g_m R \quad (12)$$

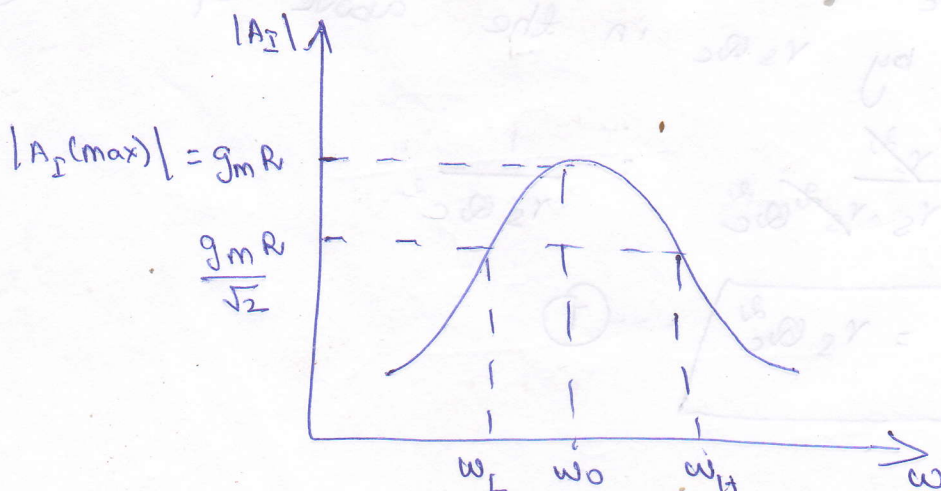


fig. Gain versus frequency of single tuned amplifier



At 3dB frequency.

$$|A_I| = \frac{g_m R}{\sqrt{2}} \quad \dots (13)$$

Similarly, at 3dB frequency.

$$1 + jQ \left[ \left( \omega / \omega_0 \right) - \left( \omega_0 / \omega \right) \right] = \sqrt{2}.$$

$$1 + Q^2 \left[ \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right]^2 = 2 \quad \dots (14)$$

The above equation is quadratic in  $\omega$  and has two positive solutions  $\omega_H$  and  $\omega_L$ . After solving the above equation we get 3dB bandwidth as

$$BW = f_H - f_L = \frac{\omega_0}{2\pi Q} = \frac{1}{2\pi RC}$$

$\therefore \text{Bandwidth} = \frac{1}{2\pi RC} \quad \dots (15)$

Problem:- Design a single tuned amplifier for following specification, centre frequency = 500kHz and Bandwidth = 10kHz. Assume transistor parameters  $g_m = 0.04 \text{ S}$ ,  $h_{fe} = 100$ ,  $C_{b'e} = 1000 \text{ pF}$  and  $C_{b'c} = 100 \text{ pF}$ . The bias network and the input resistance are adjusted so that  $r_i = 4 \text{ k}\Omega$  and  $R_L = 510 \Omega$ .

Sol:-

we know that  $\Rightarrow BW = \frac{1}{2\pi RC} \quad \dots (1)$

$$\therefore RC = \frac{1}{2\pi BW} = \frac{1}{2 \times 3.14 \times 10 \times 10^3} = 15.91 \times 10^{-6} \quad \dots (2)$$

from the single tuned amplifier circuit

$$R = r_i \parallel R_P \parallel r_{b'e} \quad \text{--- (3)}$$

where  $r_i = 4 \text{ k}\Omega$  ;  $r_{b'e} = \frac{h_{ie}}{g_m} = \frac{100}{0.04} = 2500$

$$R_P = \frac{Q_c}{\omega_0 C} = \frac{Q}{500 \times 10^3 \times C} \quad \text{--- (4)}$$

from (2) we can write.

$$C = \frac{1}{2\pi B.W. R} = \frac{1}{2 \times 3.14 \times 10 \times 10^3 \left[ 4 \times 10^3 \parallel 2500 \parallel \frac{Q_c}{2 \times 500 \times 10^3 \times C} \right]}$$

$$C = \frac{1}{2 \times 3.14 \times 10^4 \left[ 1538.5 \parallel \frac{1}{2 \times 500 \times C} \right]}$$

$$= \frac{1}{6.28 \times 10^4 \left[ \frac{1}{1538.5} + 2 \times 500 \times C \right]}$$

$$= \frac{1}{6.28 \times 10^4 \left[ \frac{1538.5}{1 + 48.3 \times 10^6 C} \right]} = \frac{9.66 \times 10^7}{(1 + 48.3 \times 10^6 C)}$$

$$C = \frac{1 + 48.3 \times 10^6 C}{96.6 \times 10^6} \Rightarrow 96.6 \times 10^6 C = 1 + 48.3 \times 10^6 C$$

$$96.6 \times 10^6 C - 48.3 \times 10^6 C = 1$$

$$48.3 \times 10^6 C = 1$$

$$C = \frac{1}{48.3 \times 10^6} = 0.02 \times 10^{-6}$$

$$\Rightarrow \boxed{C = 0.02 \mu F}$$



For hybrid  $\pi$  equivalent circuit.

$$C = C' + C_{b'e} + (1 + g_m R_L) C_{b'c}$$

$$C' = C - [C_{b'e} + (1 + g_m R_L) C_{b'c}]$$

$$= 0.02 \times 10^{-6} - [1000 \times 10^{-12} + (1 + 0.04 \times 510) \times 100 \times 10^{-12}]$$

$$C' = 0.02 \mu F$$

we know that

$$\omega_0^2 = \frac{1}{LC}$$

$$\Rightarrow L = \frac{1}{\omega_0^2 C}$$

$$\therefore L = \frac{1}{[2 \times 3.14 \times 500 \times 10^3]^2 \times 0.02 \times 10^{-6}} = 5 \times 10^{-6} H$$

Now we can find the value of  $R_p$

$$R_p = \omega L R_c = 2 \times 3.14 \times 500 \times 10^3 \times 5 \times 10^{-6} \times 100 = 1570 \Omega$$

$$\therefore R = r_i \parallel R_p \parallel r_{b'e}$$

$$= 4 \times 10^3 \parallel 1570 \parallel 2500$$

$$R = 777 \Omega$$

Mid frequency gain can be written as

$$A_i(\max) = -g_m R$$

$$= -(0.04) (777)$$

$$A_i(\max) = -31$$



## Neutralization Method :-

In tuned amplifiers, transistors are used at the frequencies nearer to their unity gain bandwidth, to amplify a narrow band of high frequencies between base and collector.  $C_{bc}$  of the transistor becomes dominant, centered around a radio frequency. At this frequency, the inter junction capacitance between base and collector,  $C_{bc}$  of the transistor becomes dominant.

In a CE configuration circuit capacitance  $C_{bc}$ , shown in below circuit appears between input and output circuit of an amplifier.

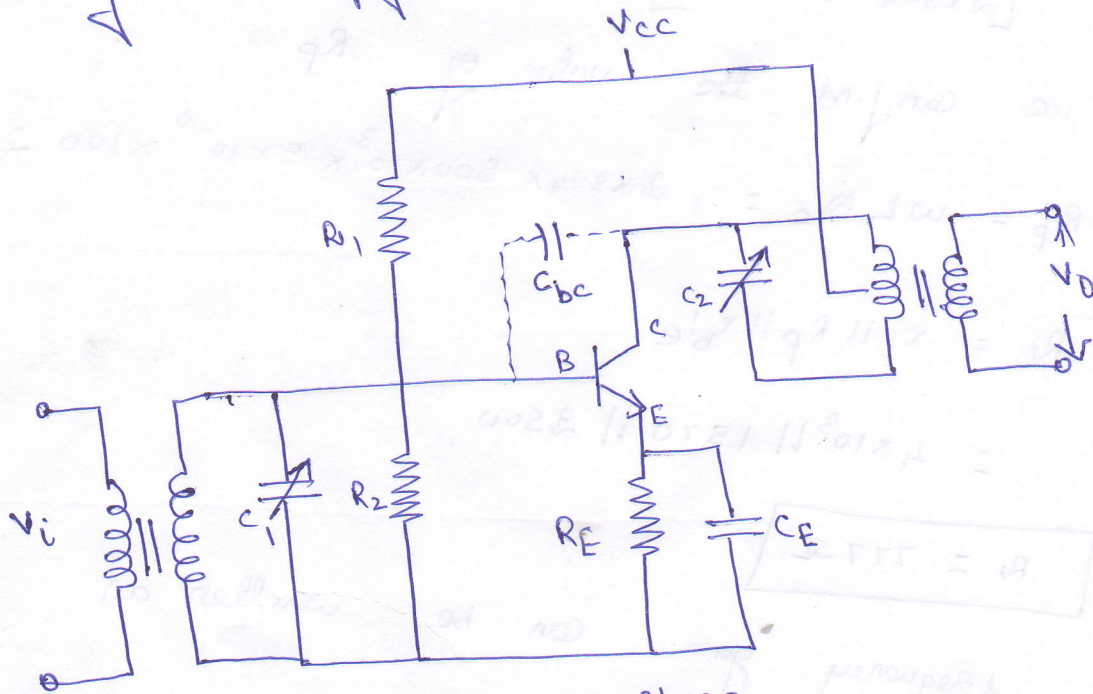


Fig. Tuned RF Stage.

As reactance of  $C_{bc}$  at RF is low enough it provides the feedback path from collector to base. Under this condition, if some feedback signal manages,

to reach the input from output in a positive manner with proper phase shift then there is possibility of circuit converted to an unstable one, generating its own oscillation and can stop working as an amplifier.

In order to prevent oscillation in tuned RF circuit amplifier it was necessary to reduce the stage gain to a level that ensured circuit stability. This could be accomplished in several ways such as lowering the  $Q$  of tune circuits, stagger tuning, loose coupling between the inserting a 'loss' element into the circuit.

Instead of losing the circuit performance to achieve stability, the pro. L.A. Hazeltine introduced a circuit performance ~~to achieve stability~~, in which the troublesome effect of the collector to base capacitance of the transistor was neutralized by introducing a signal which cancels the signal coupled through the collector to base capacitance.

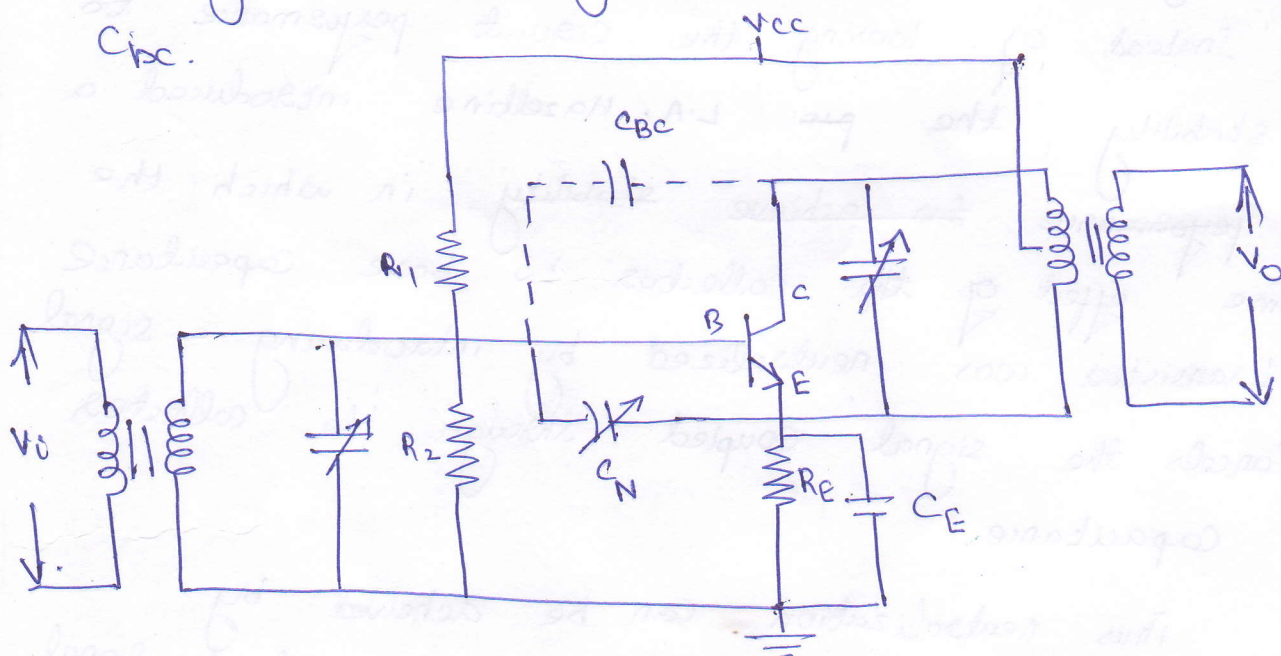
Thus neutralization can be achieved by deliberately feeding back a portion of the output signal to the input in such a way that it has the same amplitude as the unwanted feedback but the opposite phase. Various types of neutralization are namely.

- (i) Hazeltine Neutralization
- (ii) Modified hazeltine Neutralization.
- (iii) Neutralization using coil.



## (i) Hazeltine Neutralization:

In hazeltine neutralization circuit a small value of variable capacitance  $C_N$  is connected from the bottom of the coil (transformer primary through emitter to base). Therefore the internal capacitance  $C_{bc}$  feeds signal from the top end of the coil, to the transistor base and  $C_N$  feed a signal of equal magnitude but opposite polarity from the bottom of coil to the base. So the neutralizing capacitor,  $C_N$  can be adjusted correctly to completely nullify the signal fed through the  $C_{bc}$ .



## (ii) Modified Hazeltine (Neutrodyne) Neutralization:

In modified neutralization method the capacitor  $C_N$  is connected from the lower end of the base coil of the next stage to the base of the transistor.



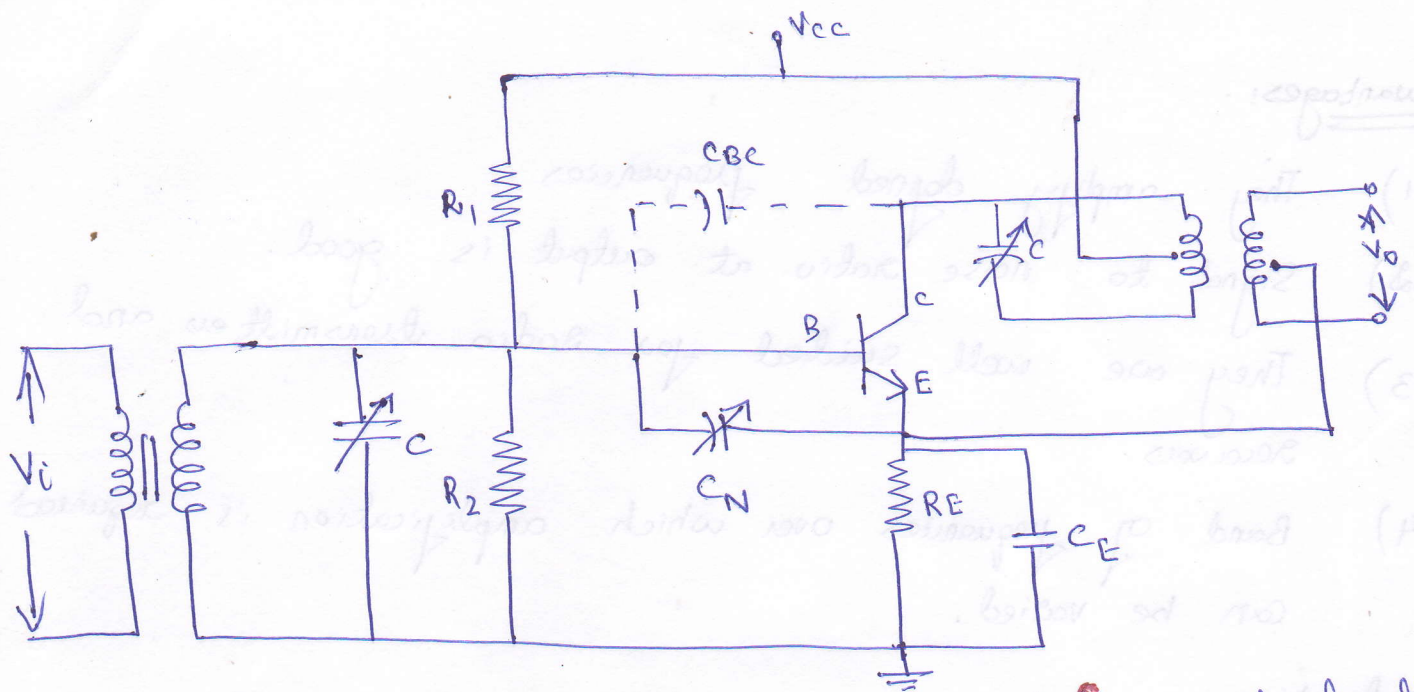


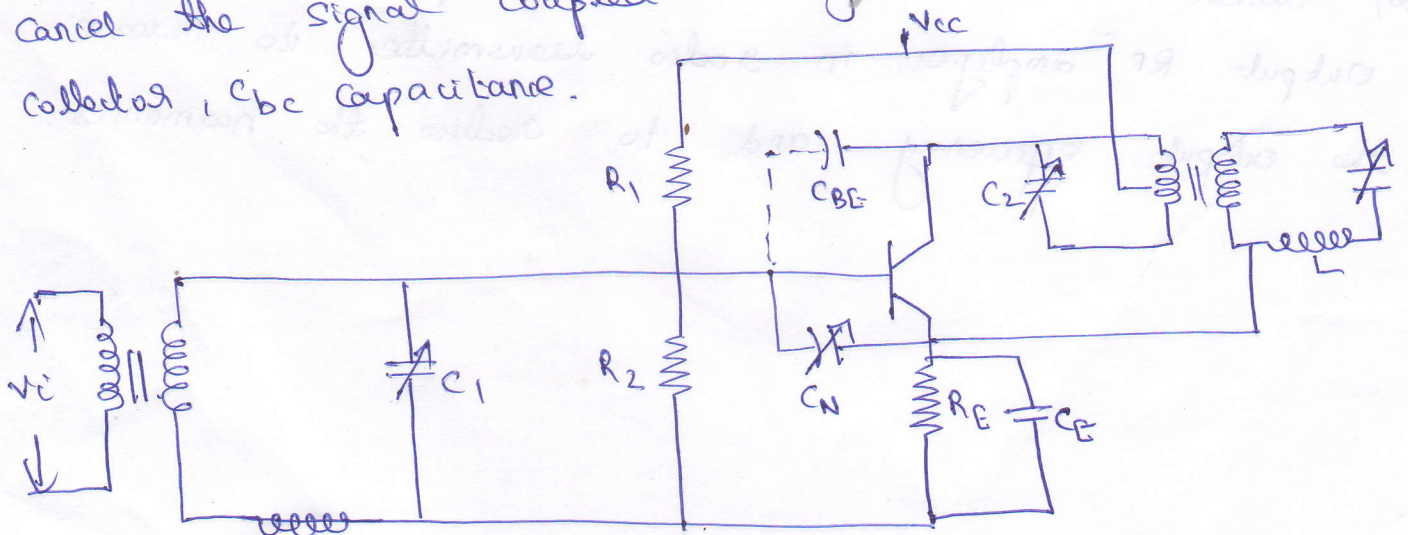
Fig. Tuned amplifier with neutralization.

Here neutralizing capacitance does not have supply voltage across it.

### iii) Neutralization using Coil:-

In the neutralization circuit using coil where  $L$  part of the tuned circuit at the base of next stage is oriented for minimum coupling to the other windings.

If the windings are properly polarized the voltage across  $L$  due to the circulating current in the base circuit will have the proper phase to cancel the signal coupled through the base to collector,  $C_{bc}$  capacitance.



### Advantages:

- 1) They amplify desired frequencies
- 2) Signal to noise ratio at output is good.
- 3) They are well suited for radio transmitters and receivers.
- 4) Band of frequencies over which amplification is required can be varied.

### Disadvantage:-

- 1) Since it uses inductors and capacitors as tuning elements, the circuit is bulky and costly.
- 2) If band of frequency increased, design becomes complex.
- 3) It is not suitable to amplify audio frequency.

### Application:-

- 1) Tuned amplifiers are used in radio receiver to amplify a particular band of frequencies for which the radio receiver is tuned.
- 2) Tuned class B and class C amplifiers are used as an output RF amplifier in radio transmitter to increase the output efficiency and to reduce the harmonics.



## Power Amplifiers [Large Signal Amplifier]

The system consists of many stages connected in cascade as shown below where input is sound signal of a human speaker and the output is given to the loudspeaker which is an amplified input signal.

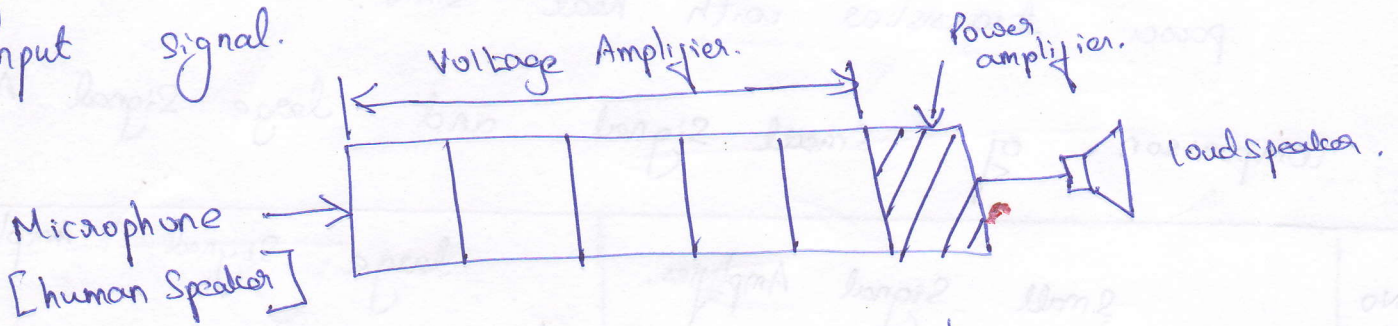


Fig. Power amplifier system.

The input and the intermediate stage are small signal amplifiers. These stages are called voltage amplifier. But last stage give an output to the load like a loud speaker. Hence the last stage must be capable of delivering an appreciable amount of a.c. power to the load.

Such a stage which develops and feeds sufficient power to the load like loudspeaker & servomotor is called large signal amplifier (or) power amplifier.

Features of large signal amplifier (Power Amplifier):

- 1) Input signal level is large of the order of few volts.



2. Output has large current and voltage swings, thus handles large power.
3. The h-parameter analysis is not applicable
4. Impedance matching with the load is required.
5. large power dissipation hence transistors used are power transistors with heat sinks.

### Comparison of Small Signal and large Signal Amplifier

| SNO | Small Signal Amplifier.                                               | large Signal Amplifier.                                            |
|-----|-----------------------------------------------------------------------|--------------------------------------------------------------------|
| 1   | Voltage is Amplified.                                                 | Power or Current is amplified.                                     |
| 2   | The h-parameter analysis is applicable.                               | The graphical analysis is required as h-parameter can not be used. |
| 3   | Harmonics are not present                                             | Harmonics are present.                                             |
| 4   | The normal transistors are sufficient                                 | The power transistors are required.                                |
| 5   | The heat sinks are not required as heat dissipation is not a problem. | The heat sink is essential                                         |
| 6   | Power handling capacity is small.                                     | Power handling capacity is large.                                  |

## Classification of Power amplifier :-

The position of the quiescent point on the load line decides the class of operation of the power amplifier. The various classes of power amplifier are namely.

- (i) class A    (ii) class B    (iii) class C    (iv) class AB

### class A Amplifier :-

The power amplifier is said to be class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input signal.

Types of class A power amplifier.

- (i) Direct coupled.  
(ii) Transformer coupled.

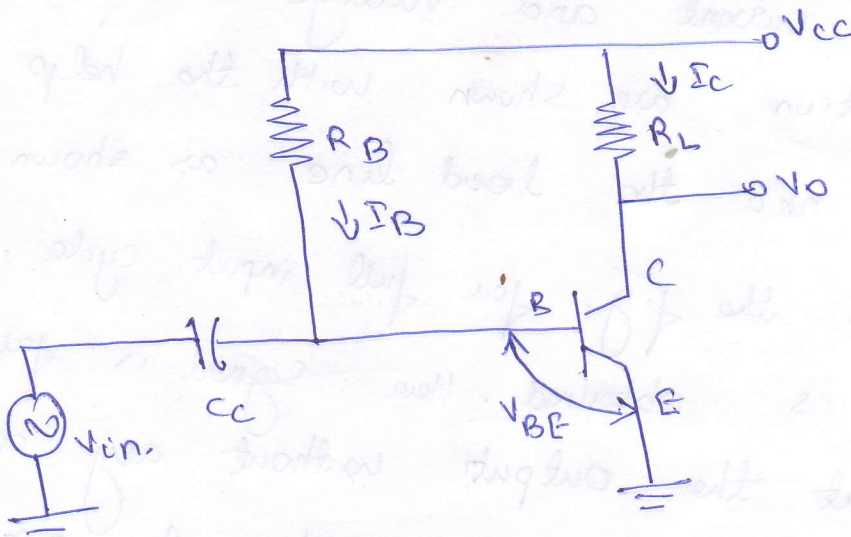


Fig. Direct Coupled class A amplifier.



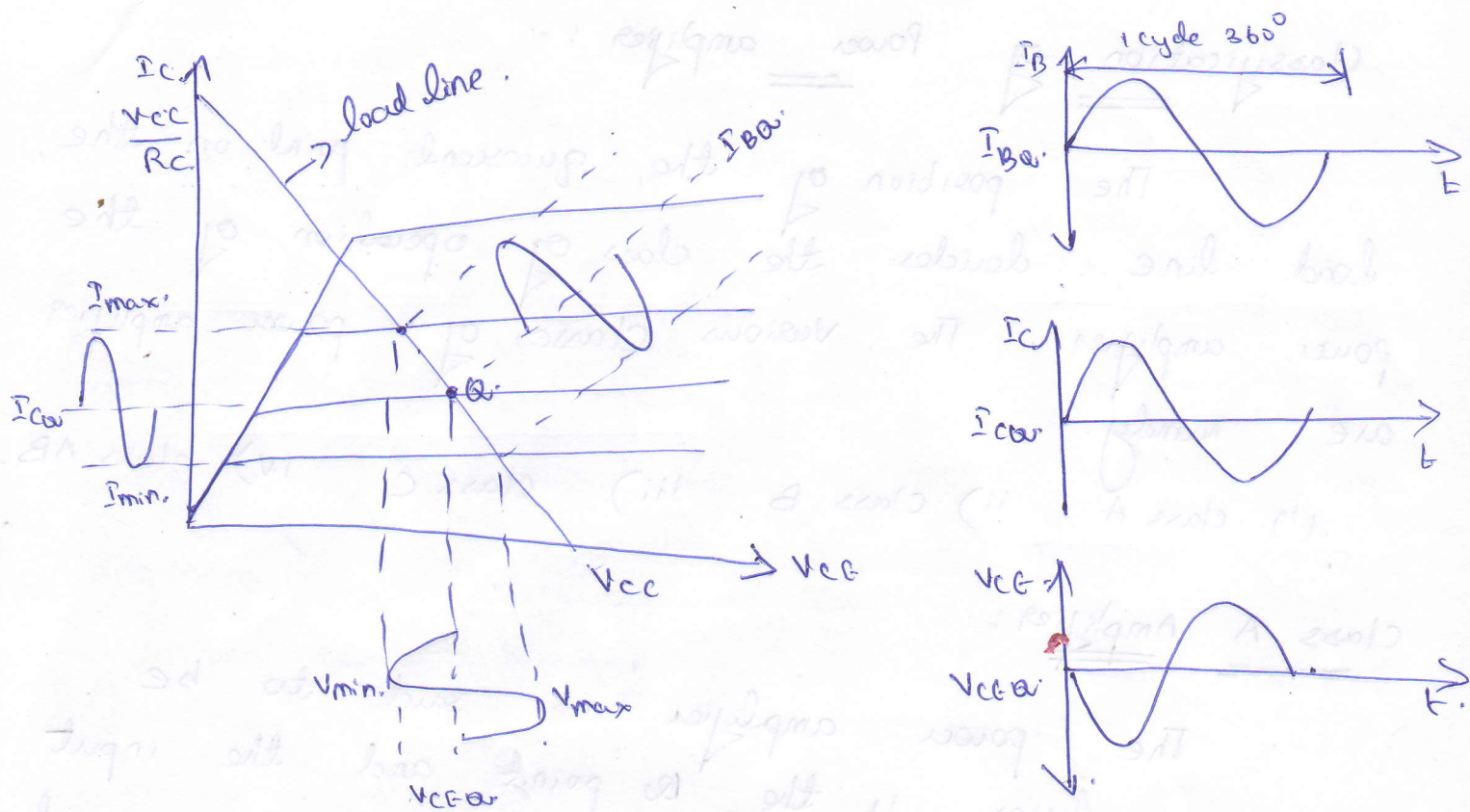


Fig. wave form representation of class A operation.

For all values of input signal, the transistor remains in the active region and never enters into cut off (or) saturation region.

The current and voltage waveforms for a class A operation are shown with the help of output characteristic and the load line as shown above.

From the fig. for full input cycle, a full output cycle is obtained. Here signal is faithfully reproduced at the output without any distortion. This is an important feature of class A operation.



The efficiency of class A operation is very small lies between 25 % to 50 %.

## Class B power amplifier:

The power amplifier is said to be class B amplifier if the Q point and the input signal are selected such that output signal is obtained only for one half cycle for a full input signal.

Types of class-B amplifier are namely.

(i) class-B : push pull amplifier.

(ii) class-B - Complementary symmetry amplifier.

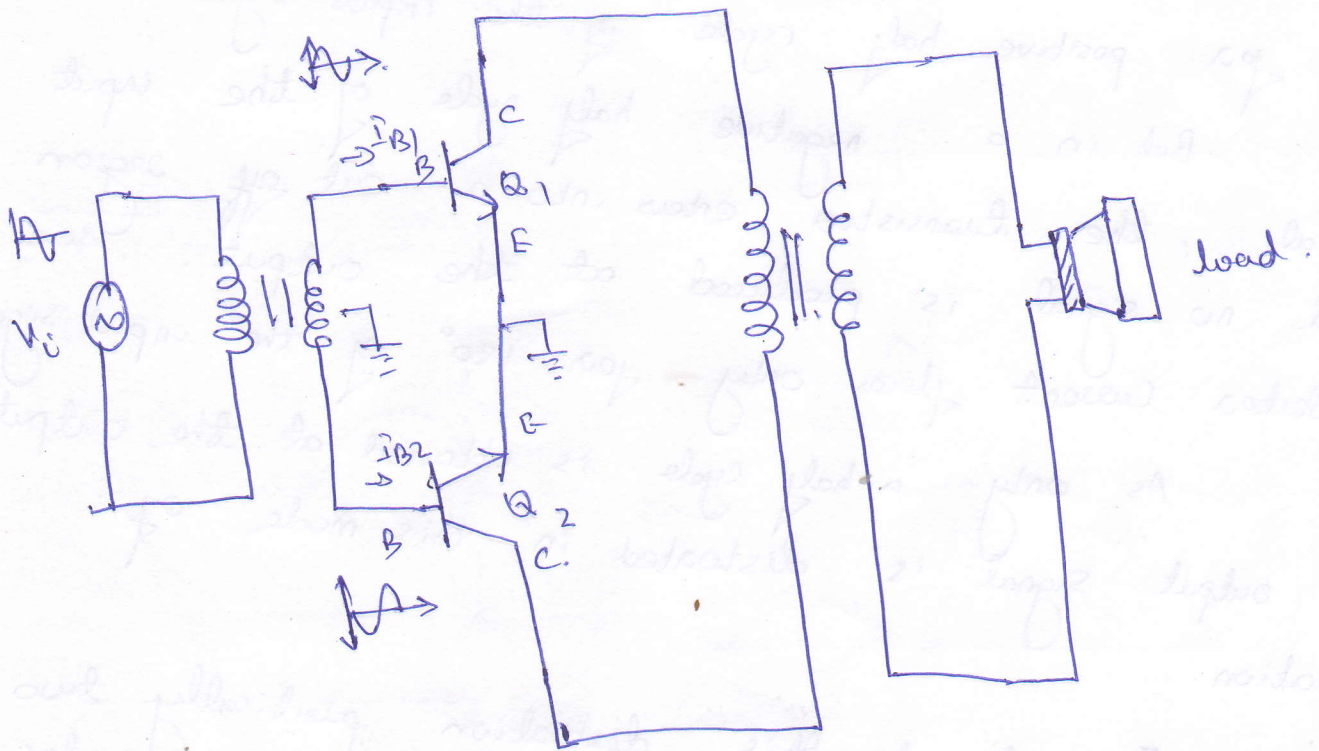


fig. Push Pull Class B power amplifier.

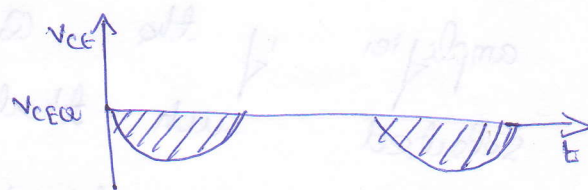
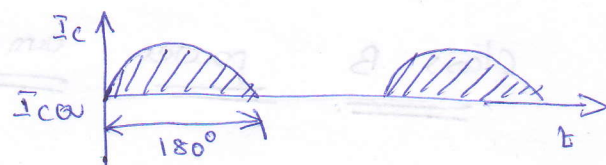
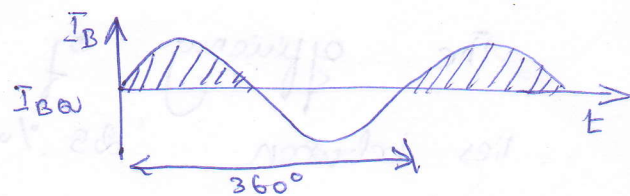
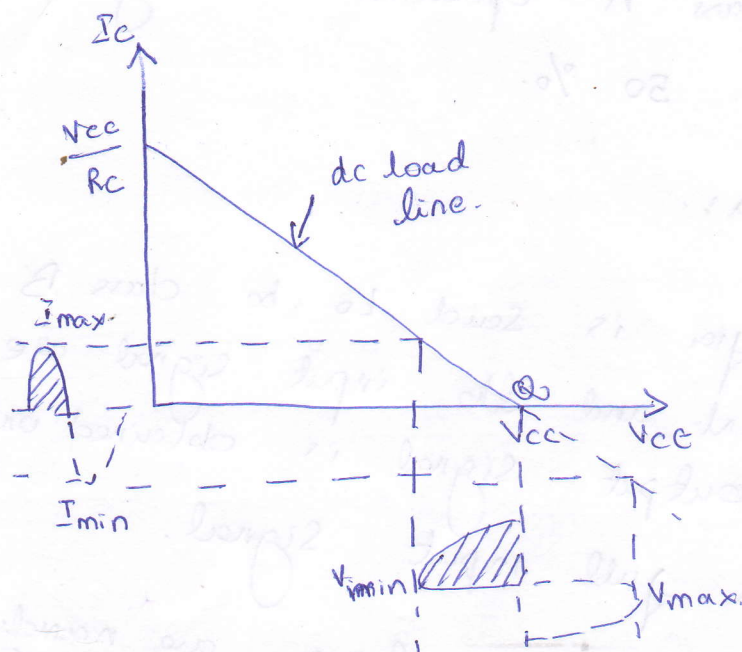


fig. waveform representation of Class B amplifier.

Due to the selection of Q point on the x-axis the transistor remains in the active region only for a positive half cycle of the input signal.

But in a negative half cycle of the input signal, the transistor enters into a cut off region and no signal is produced at the output. Here collector current flows only for 180° of the input signal.

As only a half cycle is obtained at the output, the output signal is distorted in this mode of operation.

To eliminate this distortion practically two transistors are used in the alternate half cycles of the input signal. Each transistor conducts only for a half cycle of the input signal.



The efficiency of class B amplifier is much higher than class A operation upto 78.5%.

### Class C power amplifier:-

The power amplifier is said to be class C amplifier, if the Q point and the input signal are selected such that the output signal is obtained for less than a half cycle for full input signal.

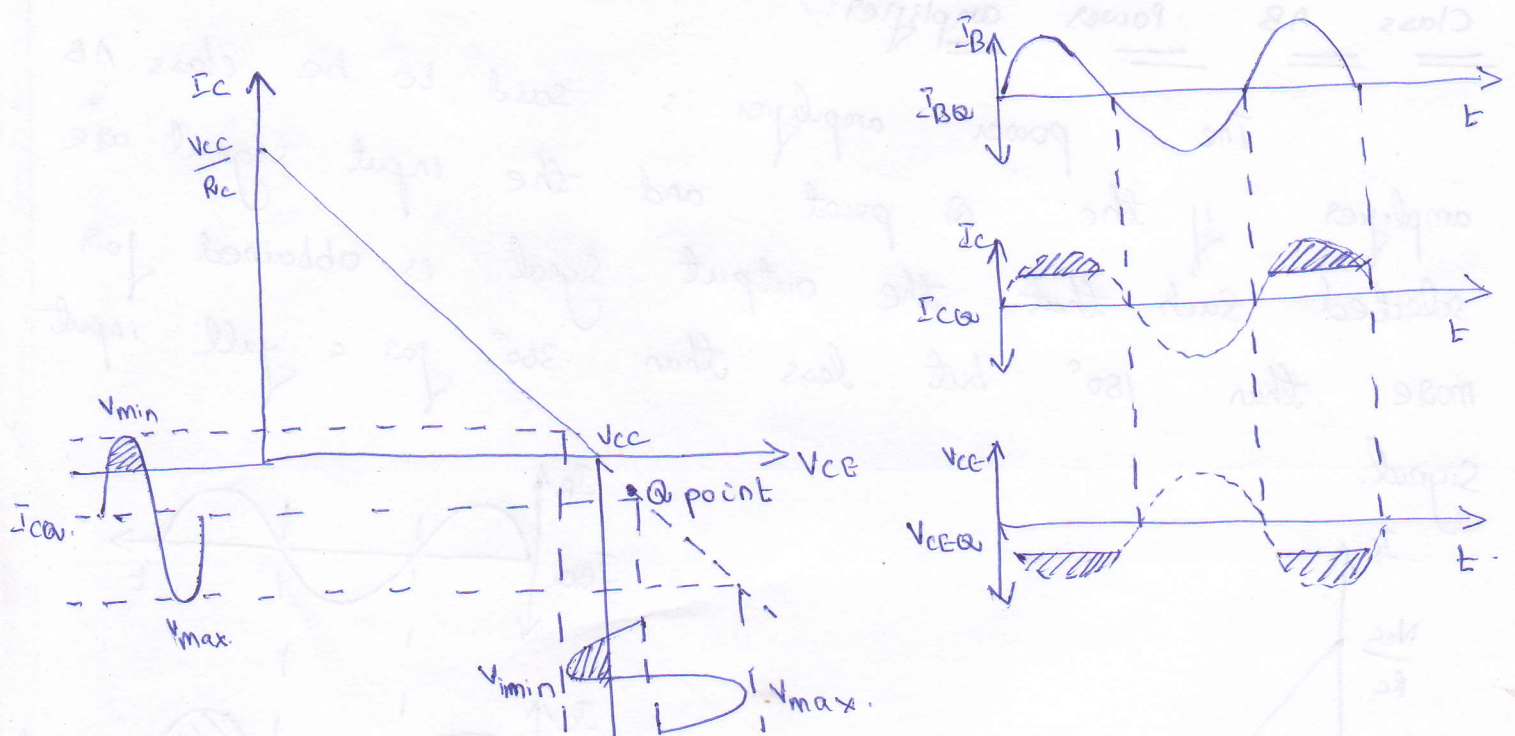


fig. Waveform representation of class C operation.

Due to such a selection of the Q-point, transistor remains active for less than a half cycle. Hence only those interval output is produced.

For remaining cycle of the input, transistor remains in cut off and no signal produced at the output.



Hence the collector current flows less than  $180^\circ$ .  
 But efficiency of class C operation is much higher  
 and can reach very close to 100 %

The class C amplifier are used in tuned  
 circuits which are used in communication area and  
 radio frequency circuits. These are also used in mixer,  
 radio receivers and wireless communication circuits.

### Class AB power amplifier:-

The power amplifier is said to be class AB  
 amplifier if the  $Q$  point and the input signal are  
 selected such that the output signal is obtained for  
 more than  $180^\circ$  but less than  $360^\circ$  for a full input  
 signal.

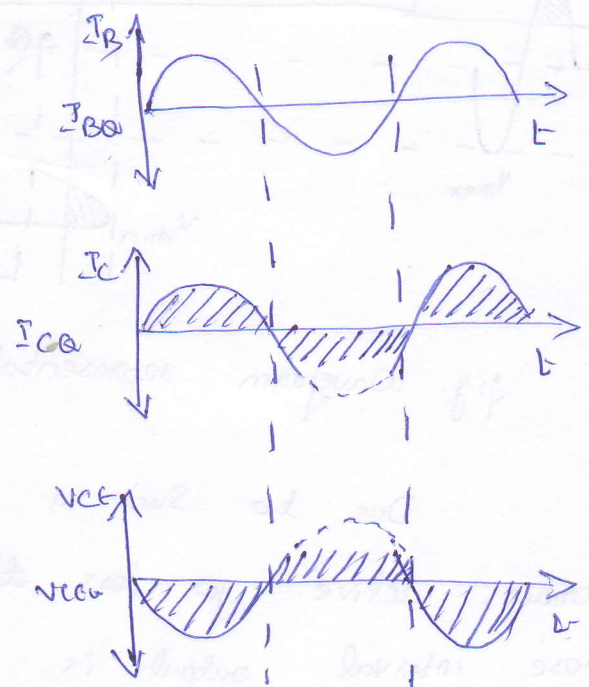
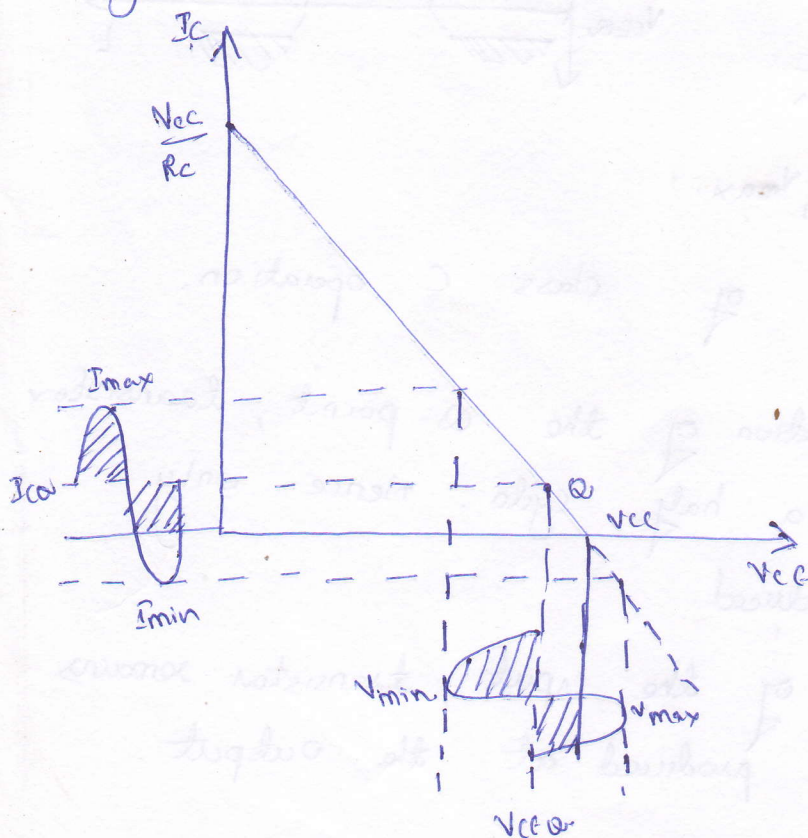


Fig. Waveform representation  
 of class AB amplifier.

Due to the selection of such Q-point, transistor remains active for more than a half cycle but less than  $360^\circ$ .

The current and voltage waveform for a class AB amplifier is shown above. Here transistor conducts for full positive half cycle and part of negative half cycle. The efficiency of class AB amplifier is more than class A but less than class B amplifier.

Class AB operation is important to eliminate cross over distortion. Due to this advantage class AB amplifier is used in audio system, radio receiver and TV receivers. etc.

### Comparison of Amplifier Classes :-

| Property -             | Class A             | Class B                   | Class C               | Class AB                                        |
|------------------------|---------------------|---------------------------|-----------------------|-------------------------------------------------|
| Collector Current flow | $360^\circ$         | $180^\circ$               | less than $180^\circ$ | more than $180^\circ$ but less than $360^\circ$ |
| Position of Q Point    | Centre of load line | On X-axis                 | Below X-axis          | Above X-axis but below the centre of load line. |
| Efficiency             | 25% to 50%          | 78.5%                     | High                  | 50% to 78%                                      |
| Distortion             | No distortion       | Present more than class A | Highest               | Present                                         |



Power dissipation in transistor.

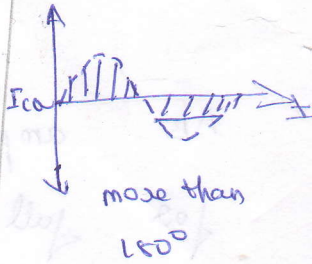
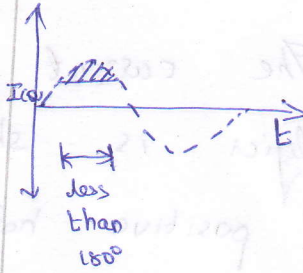
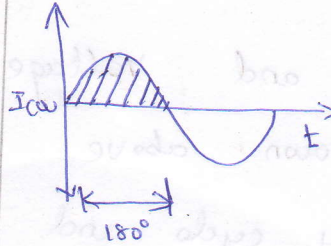
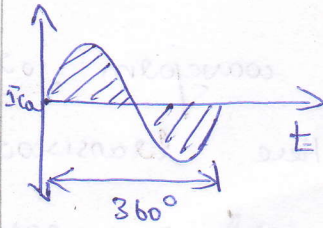
very high

low

very low

Moderate

Nature of output current wave form.



Class AB amplifier is important to eliminate crossover distortion. The to this advantage class AB amplifier is used in audio system, radio receiver and TV set.

Comparison of amplifier classes

| Class A                         | Class B   | Class C        | Class AB                          |
|---------------------------------|-----------|----------------|-----------------------------------|
| Collector current flows only    | 180°      | less than 180° | more than 180° but less than 360° |
| Location of point of no current | On x-axis | Below x-axis   | Above x-axis                      |
| Efficiency 92% to 95%           | 78.2%     | High           | 50% to 78.2%                      |
| No distortion                   | present   | High           | Present                           |



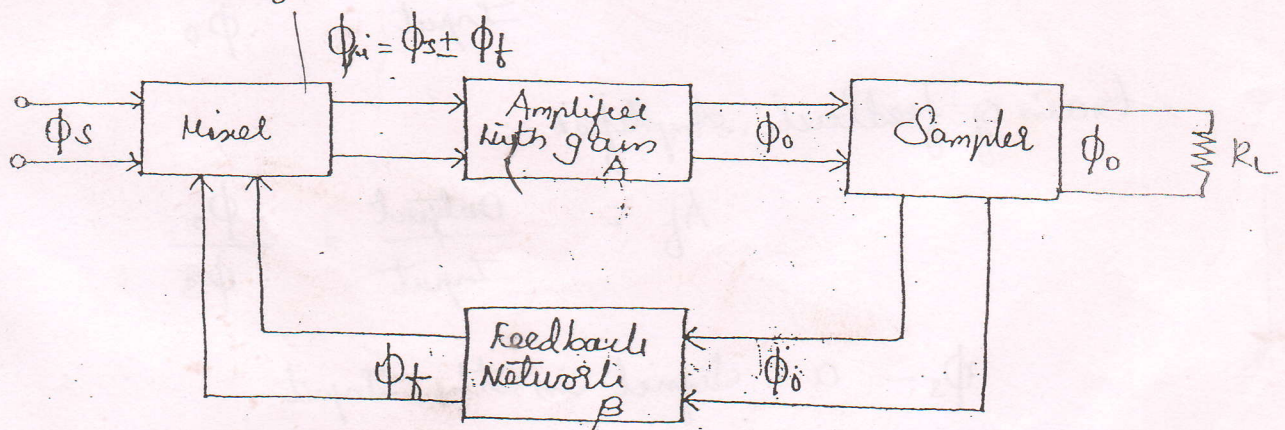
## Amplifiers and oscillators

Introduction

Feed back plays a very important role in electronic circuits and the basic parameters such as

- (i) Input & output impedance
- (ii) Current or Voltage gain
- (iii) Bandwidth, may be altered by the use of feedback.

Feedback is defined as - a part of output signal is fed to input of the circuit.

Basic Concepts of Feedback

The output quantity (either Voltage or Current) is sampled by suitable sampler.

Sampler is of two types

- (i) Voltage Sampler
- (ii) Current Sampler



From the Sampler output signal is fed to feedback

The output of feedback Network which has a fraction of output signal is combined with external source signal through a mixer and fed to basic Amplifier

Mixer is also known as Comparator

(i) Series Mixer.

(ii) Shunt Mixer.

Gain of Amplifier  $A = \frac{\text{Output}}{\text{Input}} = \frac{\phi_o}{\phi_i}$

Feedback ratio  $\beta = \frac{\text{Output}}{\text{Input}} = \frac{\phi_f}{\phi_o}$

Gain of feedback Amplifier

$$A_f = \frac{\text{Output}}{\text{Input}} = \frac{\phi_o}{\phi_s}$$

$\phi_s$  - a.c signal in the Input  
(Current / Voltage)

$\phi_f$  - feedback signal  
(Current / Voltage)



The feedback connection has three Networks

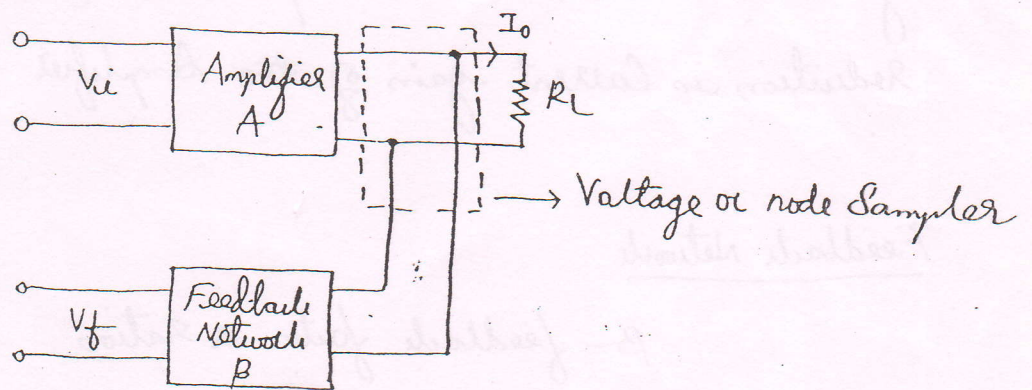
1. Sampling Network
2. Feedback Network
3. Mixer Network

Output from the basic Amplifier Voltage is Connected to the feedback network in Shunt or Series with the output.

Based on the Sampling Signal it is classified into two types

- (i) Voltage Sampling
- (ii) Current Sampling

### Voltage Sampling

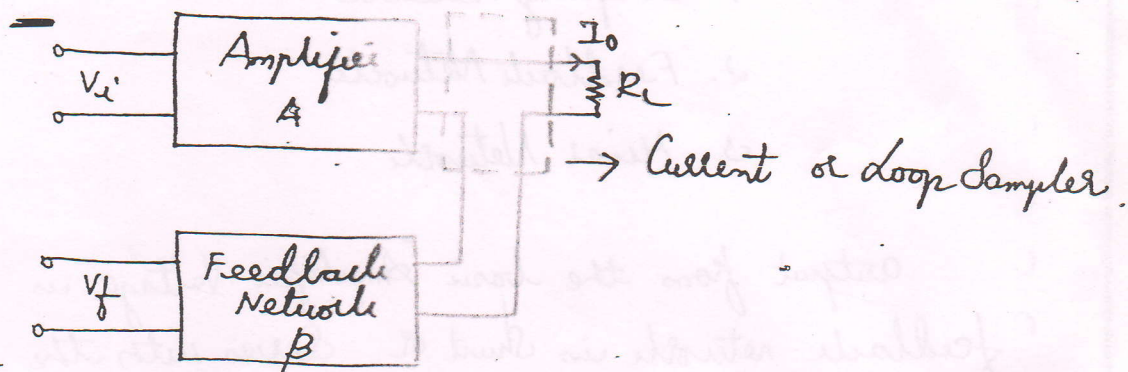


Also called as Shunt or parallel Sampler. Since the part of the output signal taken in parallel or across the load and at output of basic amplifier.

The input impedance of feedback Network must be greater than the load impedance  $R_L$  in order to avoid loading the output of the Amplifier.



## Current Sampling



Also called as loop sampling or series sampling

The sampling system samples the output current by connecting the feedback network in series with the output.

The input impedance of the feedback network must be greater than the load impedance  $R_L$  in order to avoid the reduction in current gain of the amplifier.

## Feedback Network

$\beta$  - feedback factor or ratio

$$V_f = \beta V_o$$

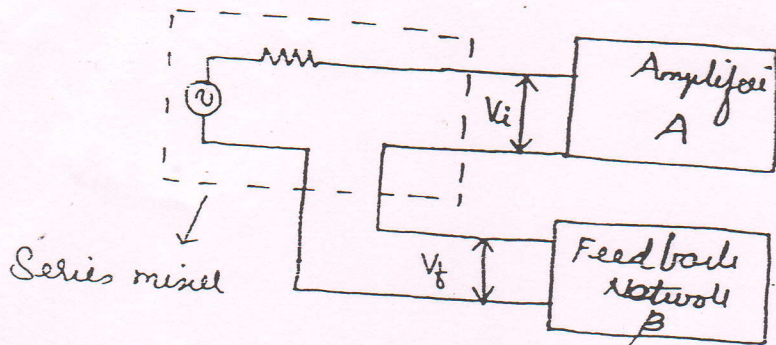
## Mixing Network

Mixer is used to mix part of output signal with input signal and then resultant signal is given to input of the amplifier.

1. Series mixing
2. Shunt mixing.



## Series Mixing

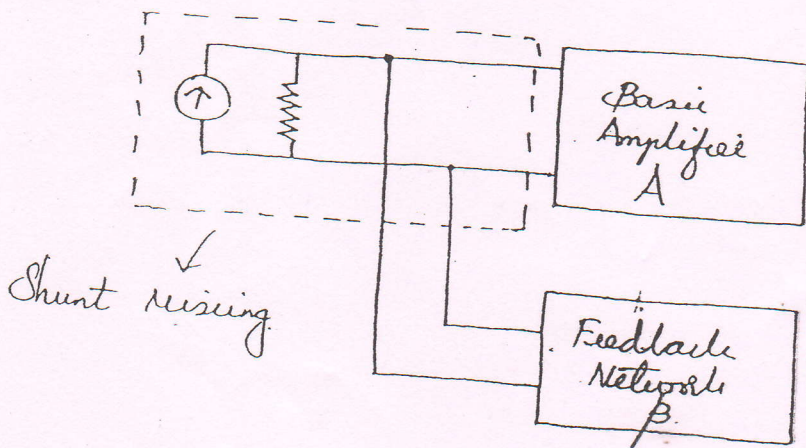


$$V_f = \beta V_o$$

The feedback signal from feedback network is mixed with input signal in series, i.e., loop formation

\* Increases the input impedance of Amplifier.

## Shunt Mixing



The feedback signal from feedback network is mixed with input signal in parallel or shunt

\* Decreases the input impedance of Amplifier.



## Types of feedback

1. Positive feedback

2. Feedback feedback.

### Positive feedback

If the feedback signal  $\phi_f$  is in phase with input signal  $\phi_s$ , then the net effect of the feedback will increase the input signal to the amplifier.

$$\text{i.e., } \phi_i = \phi_s + \phi_f$$

Hence the input voltage applied to the basic amplifier is increased,  $\therefore \phi_o$  increases.

This type of feedback is said to be positive or regenerative feedback.

Gain of the amplifier with positive feedback is  $A_f$ .

$$A_f = \frac{\phi_o}{\phi_s} = \frac{\phi_o}{\phi_i - \phi_f}$$

$$= \frac{1}{\frac{\phi_i}{\phi_o} - \frac{\phi_f}{\phi_o}} = \frac{1}{\frac{1}{A} - \beta} = \frac{A}{1 - A\beta}$$

$$A_f = \frac{A}{1 - A\beta}$$



## Negative feedback

If the feedback signal  $\phi_f$  is out of phase with the input signal  $\phi_s$  then  $\phi_i = \phi_s - \phi_f$

So the input voltage applied to the basic amplifier is decreased,  $\therefore \phi_o$  is decreased.

This type of feedback is known as Negative degenerative feedback.

Gain of the amplifier with negative feedback is  $A_f$ .

$$A_f = \frac{\phi_o}{\phi_s} = \frac{\phi_o}{\phi_i + \phi_f}$$

$$= \frac{1}{\frac{\phi_i}{\phi_o} + \frac{\phi_f}{\phi_o}} = \frac{1}{\frac{1}{A} + \beta} = \frac{A}{1 + A\beta}$$

$$\boxed{A_f = \frac{A}{1 + A\beta}}$$

- \* Positive feedback is used in Oscillators.
- \* Negative feedback is used in Amplifiers.



## Basic feedback topologies :-

The basic amplifier types are

\* Voltage amplifier

\* Current amplifier

\* Transconductance amplifier

\* Transresistance amplifier

The configuration based on <sup>sampling</sup> (i.e; current / voltage) and mixing (i.e; shunt or series) are

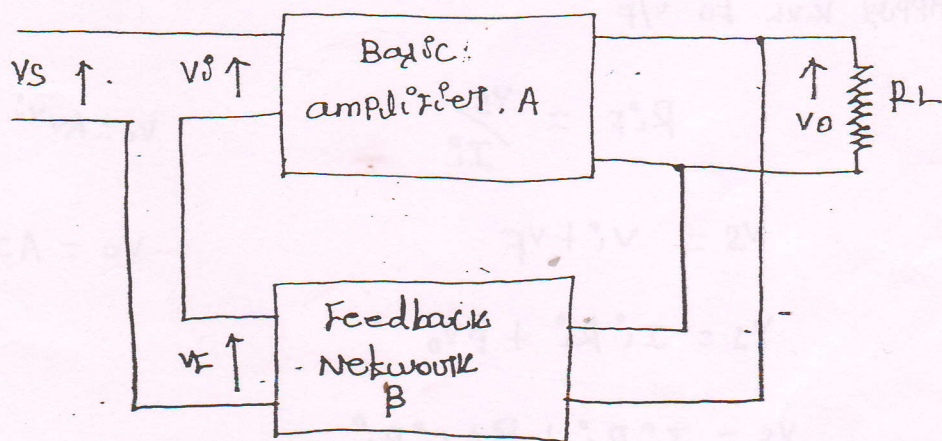
(V,V) 1 → Voltage-Series Feedback (voltage amplifier)

(I,V) 3 → Current-Series Feedback (transconductance amplifier)

(I,I) 4 → Current-Shunt Feedback (current amplifier)

(V,I) 2 → Voltage-Shunt Feedback (transresistance amplifier)

### \* Voltage-Series Feedback :-



Voltage-series feedback is also called a series shunt amplifier. The input to feedback network is in parallel with the output of the amplifier.

A fraction of output voltage through the feedback network is applied in series with the

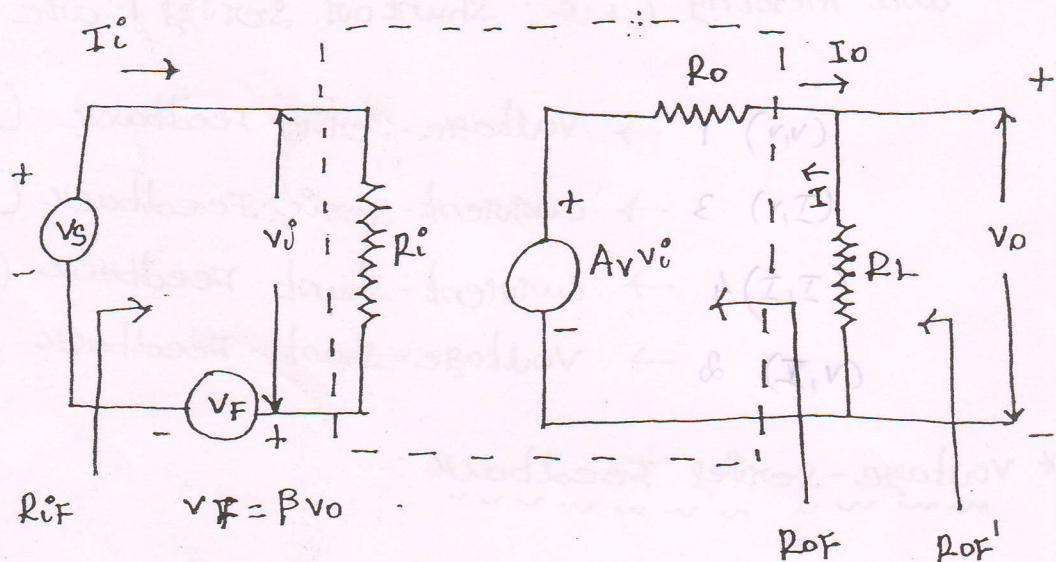


Shunt connection at the output reduces output resistance  $R_o$  and series connection at the input reduces input resistance  $R_i$ .

Voltage feedback Factor  $\beta$

$$\beta = v_F / v_o$$

Input and output resistance :-



Apply KVL to i/p

$$R_i^o = \frac{v_s}{I_i^o}$$

$$v_s = v_i + v_F$$

$$v_s = I_i^o R_i^o + \beta v_o$$

$$v_s = I_i^o R_i^o + \beta A I_i^o R_i^o$$

$$v_s = I_i^o R_i^o (1 + \beta A)$$

$$R_i^o = \frac{v_s}{I_i^o} = \frac{I_i^o R_i^o (1 + \beta A)}{I_i^o}$$

$$R_i^o = R_i^o (1 + \beta A)$$

$$v_o = A v_i$$

$$v_o = A I_i^o R_i^o$$

$$v_o = \frac{R_L}{R_o + R_L} A v_i$$

$$v_o = A v_i$$

$$v_i = I_i^o R_i^o$$

$$v_o = A I_i^o R_i^o$$



Apply KVL to output side

$$A_v V_i + I_o R_o - V_o = 0$$

$$I_o = \frac{V_o - A_v V_i}{R_o}$$

$$V_i = -V_f = -\beta V_o$$

$$I_o = \frac{V_o + A_v \beta V_o}{R_o}$$

$$I_o = \frac{V_o (1 + A_v \beta)}{R_o}$$

$$R_{of} = \frac{V_o}{I_o} = \frac{R_o}{(1 + A_v \beta)}$$

$$R_{of} = \frac{R_o}{(1 + A_v \beta)}$$

(out)

$$R_{of}' = \frac{R_o'}{(1 + A\beta)}$$

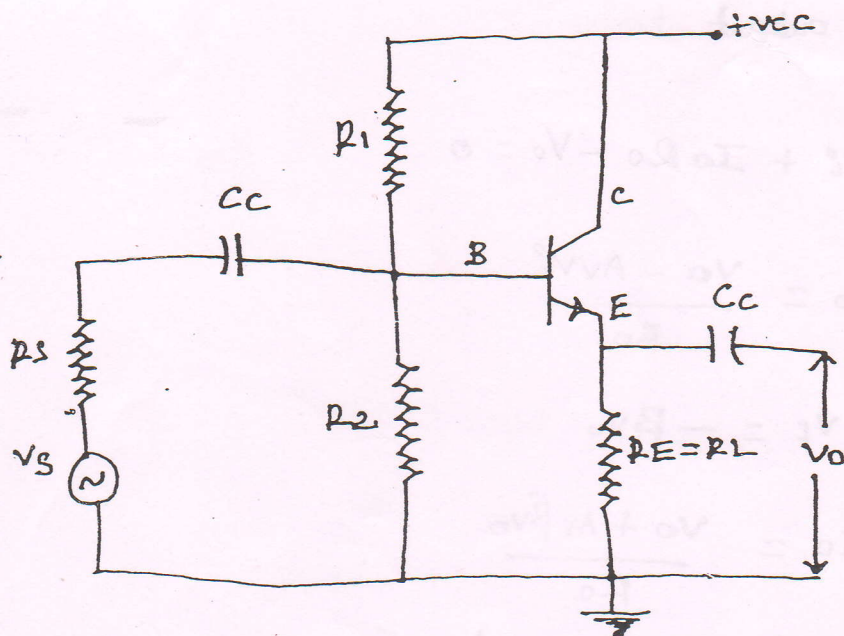
$R_o$  is the output resistance of the amplifier without feedback.

Example :- [Emitter Follower]

The common collector or emitter follower as shown in diagram. The voltage developed in the output is in series with the input voltage as far as the base-emitter junction is concerned. This is a single stage coupled amplifier without emitter bypass capacitor across  $R_E$ ,  $R_1$  and  $R_2$  provide the base bias.

— output voltage is taken across  $R_E = R_L$ , the feedback ratio,  $\beta = \frac{R_E}{R_L} \approx 1$





overall voltage gain  $A_F = \frac{A}{1+A}$ , which is little less than unity.

The emitter Follower simultaneously increases input resistance and decreases output resistance.

Characteristics of emitter Follower

$$A_i = \frac{I_e}{I_b} = \frac{I_b + I_c}{I_b} = \frac{I_b + h_{fe} I_b}{I_b} = 1 + h_{fe}$$

$$R_i = h_{ie} + (1 + h_{fe}) R_E = h_{ie} + (1 + h_{fe}) R_L$$

$$A_v = \frac{A_i R_L}{R_i} = \frac{(1 + h_{fe}) R_L}{h_{ie} + (1 + h_{fe}) R_L} = 1 - \frac{h_{ie}}{R_i} \quad - (3)$$

$$R_o = \frac{h_{ie} + R_s}{1 + h_{fe}} \quad - (4)$$

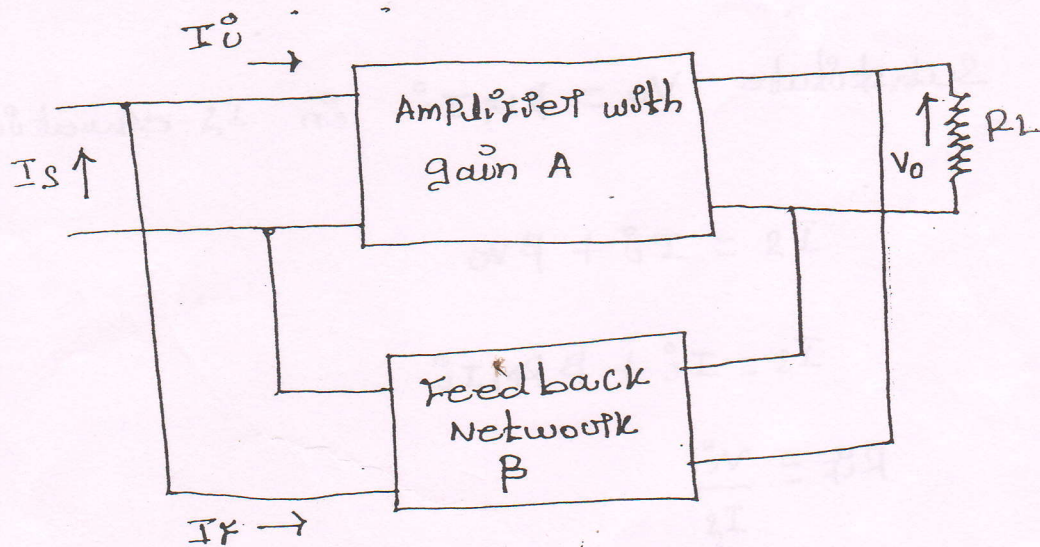
$$R_{oF} = R_o \parallel R_L \quad - (5)$$



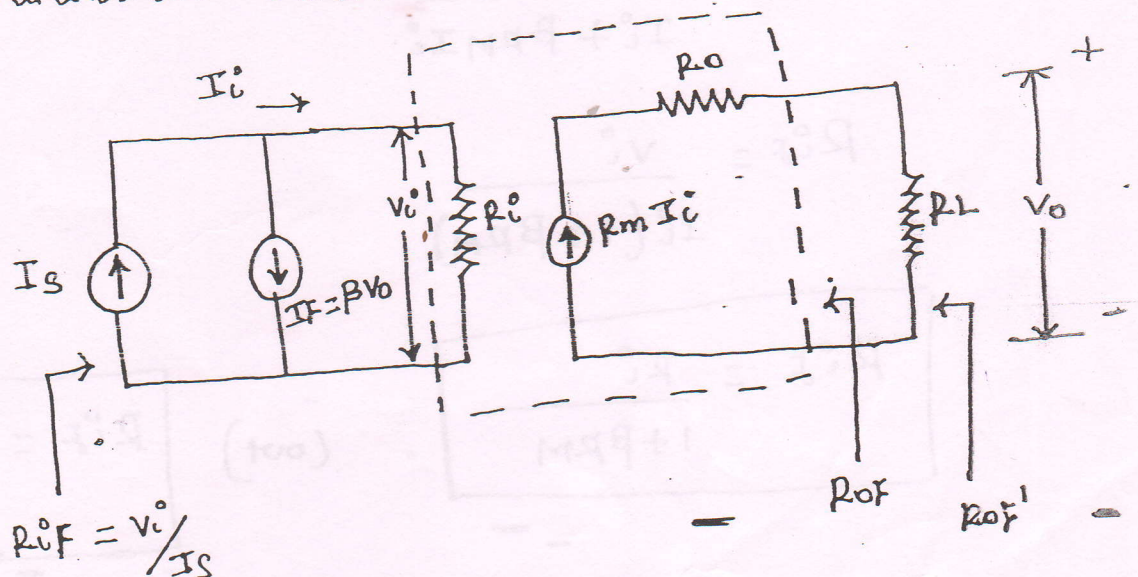
## \* Voltage-Shunt Feedback :-

The fraction of the output voltage is supplied in parallel with the input voltage through the feedback network. The feedback signal  $I_F$  is proportional to the output voltage  $V_o$ . The feedback factor is given by  $\beta = I_F / V_o$ .

This type of amplifier is called a trans-resistance amplifier.



Input and output resistance :-





Apply KCL to input side

$$I_s = I_i^o + I_f$$

$$I_s = I_i^o + \beta V_o$$

$$V_o = \frac{R_L}{R_o + R_L} R_m I_i^o$$

$$V_o = R_M I_i^o$$

$$\text{where } R_M = \frac{R_L \cdot R_m}{R_o + R_L}$$

Substitute  $V_o = R_M I_i^o$  in  $I_s$  equation

$$I_s = I_i^o + \beta V_o$$

$$I_s = I_i^o + \beta R_M I_i^o$$

$$R_{if}^o = \frac{V_i^o}{I_s}$$

$$R_{if}^o = \frac{V_i^o}{I_i^o + \beta R_M I_i^o}$$

$$R_{if}^o = \frac{V_i^o}{I_i^o (1 + \beta R_M)}$$

$$R_{if}^o = \frac{R_i^o}{1 + \beta R_M}$$

(out)

$$R_{if}^o = \frac{R_i^o}{1 + A\beta}$$

Apply KVL to output ( $I_{L20}$ ):-

$$r_m I_c + I_o R_o - V_o = 0$$

$$I_o = \frac{V_o - r_m I_c}{R_o}$$

$$I_c = -I_f = -\beta V_o$$

$$I_o = \frac{V_o + r_m \beta V_o}{R_o}$$

$$I_o = \frac{V_o (1 + r_m \beta)}{R_o}$$

$$R_{of} = \frac{V_o}{I_o}$$

$$R_{of} = \frac{R_o \cdot V_o}{V_o (1 + r_m \beta)}$$

$$R_{of} = \frac{R_o}{1 + r_m \beta}$$

(out)

$$R_{of} = \frac{R_o}{1 + A\beta}$$

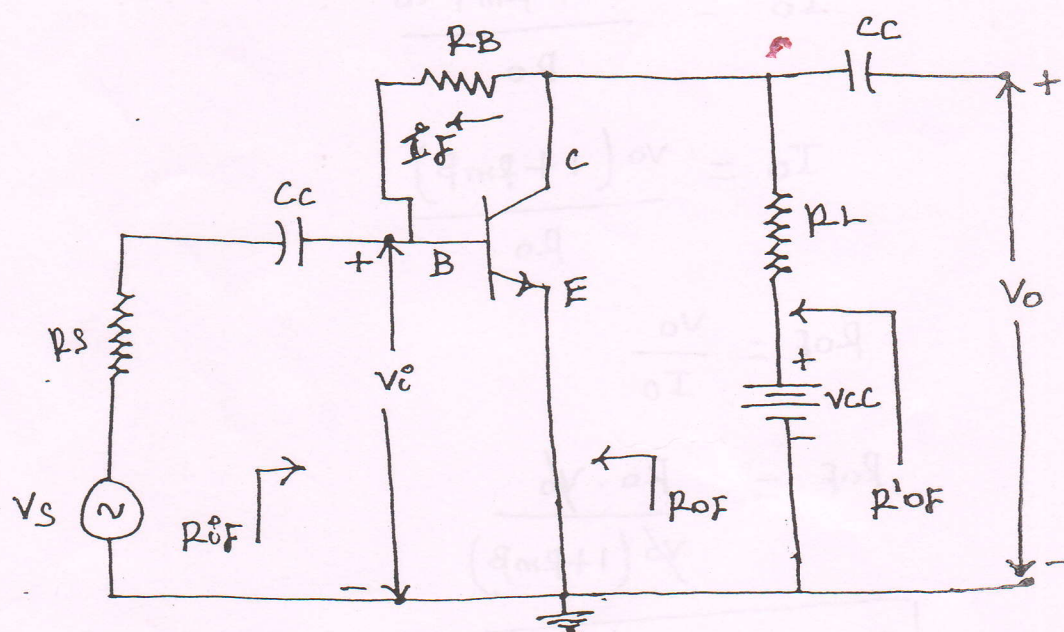
$$R_{of}' = \frac{R_o'}{1 + A\beta}$$



E.T:-

Common emitter amplifier with voltage shunt feedback :-

The current which is proportional to the output voltage is feedback to the input. Since the feedback current  $I_F = \frac{V_o}{R_B}$ , so that the feedback ratio  $\beta = \frac{1}{R_B}$



The reduction in input and output resistances occurred to Miller effect with  $R_B$

$$R_{iF} = h_{ie} \parallel \frac{R_B}{1 - A_v} \quad \text{where } A_v = \frac{V_o}{V_i} = -\frac{h_{fe} R_L}{h_{ie}}$$

$$\text{and } R_L' = R_B \parallel R_L \quad \text{--- (2)}$$

$$A_{vF} = \frac{V_o}{V_s} = A_v \frac{R_{iF}}{R_s + R_{iF}} \quad \text{--- (3)}$$

$$R_{oF} = \frac{R_B}{R_s} \times \frac{R_s + h_{ie}}{h_{fe}} \quad \text{--- (4)}$$

$$R_{oF}' = R_{oF} \parallel R_L$$

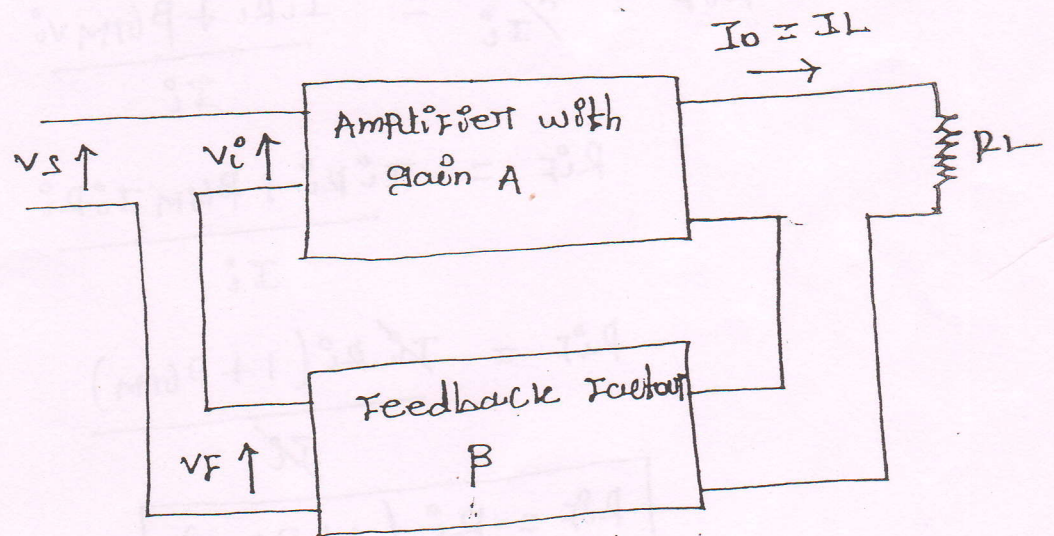


## \* Current-Series Feedback :-

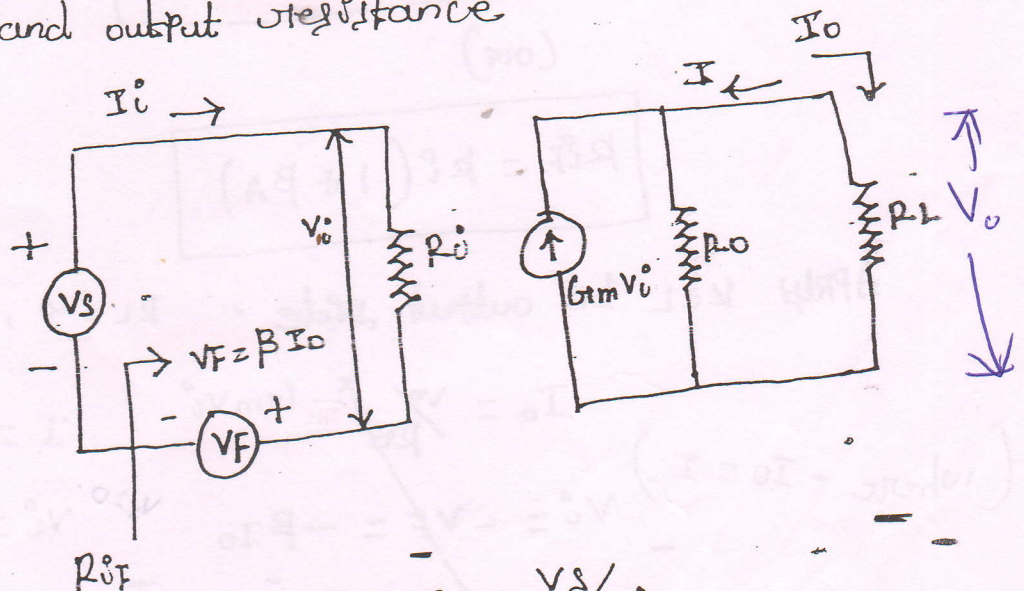
In current-series feedback, a voltage developed which is proportional to the output current this is called current feedback even though it is a voltage that subtracts from the input voltage.

This type of amplifier is called transconductance

the transconductance feedback factor or ratio is given by  $\beta = V_F / I_O$



Input and output resistance



$$I + G_m V_i = \frac{V_o}{R_o}$$

$$I = \frac{V_o}{R_o} - G_m V_i$$

$$\therefore R_{if} = \frac{V_s}{I_i}$$



Apply KVL to input side

$$V_s - I_i R_i - V_F = 0$$

$$V_s = I_i R_i + V_F$$

$$V_s = I_i R_i + \beta I_o$$

$$I_o = \frac{R_o}{R_o + R_L} \cdot G_m V_i$$

$$I_o = G_m V_i$$

$$\text{where } G_m = \frac{R_o}{R_o + R_L} \cdot G_m$$

$$R_{if} = V_s / I_i = \frac{I_i R_i + \beta G_m V_i}{I_i}$$

$$R_{if} = \frac{I_i R_i + \beta G_m I_i R_i}{I_i}$$

$$R_{if} = \cancel{I_i} R_i (1 + \beta G_m) / \cancel{I_i}$$

$$R_{if} = R_i (1 + \beta G_m)$$

(out)

$$R_{if} = R_i (1 + \beta A)$$

Apply KCL to output side -  $R_L = \infty$ , replace  $v_o$  with  $v_{s20}$

$$I_o = \cancel{v_o / R_o} - G_m V_i$$

$$I = \cancel{v_o / R_o} - G_m V_i$$

(where  $-I_o = I$ )

$$V_i = -V_F = -\beta I_o = \beta I$$

$$V_i = -V_F = -\beta I_o = \beta I$$

$$I = \cancel{v_o / R_o} - \beta G_m I$$

$$I_o = \cancel{v_o / R_o} - G_m \beta I_o$$



$$I_o(1 + \beta g_m) = V_o / R_o$$

$$I(1 + \beta g_m) = V / R_o$$

$$R_{of} = V_o / I_o$$

$$R_{of} = V / I$$

$$R_{of} = R_o(1 + \beta g_m)$$

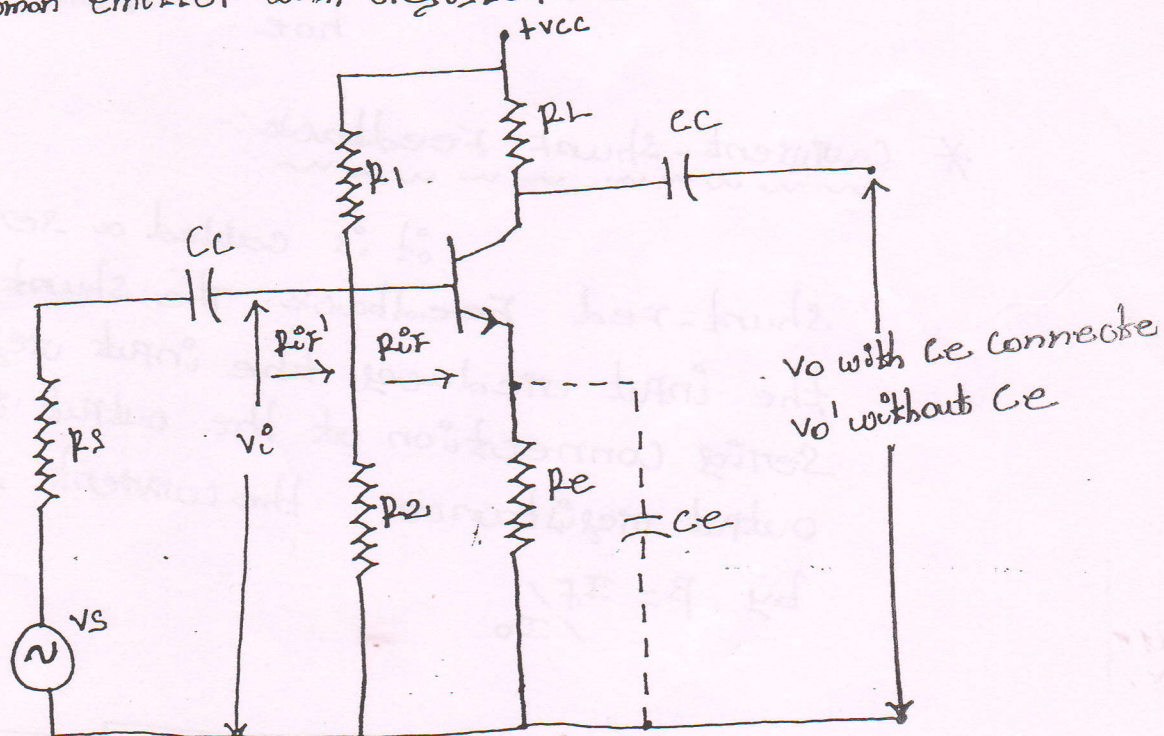
$$\therefore R_{of} = R_o(1 + \beta g_m)$$

(or)

$$R_{of} = R_o(1 + A\beta)$$

E.x:-

Common emitter with resistor  $R_e$  when  $C_e$  is removed.



$$R_{i'} = R_i + (1 + \beta r_e) R_e \quad \text{--- (1)}$$

input resistance without feedback  $R_s = h_{ie}$  --- (2)

$$R_{i'} = h_{ie} + (1 + \beta r_e) R_e$$

The effective input resistance with feedback

$$R_{of}' = R_s \parallel R_{i'}$$



Voltage gain ( $A_F$ ) :-

$$A_F = \frac{A_i R_L}{R_{iF}} \quad \text{and} \quad A_i = -h_{fe}$$

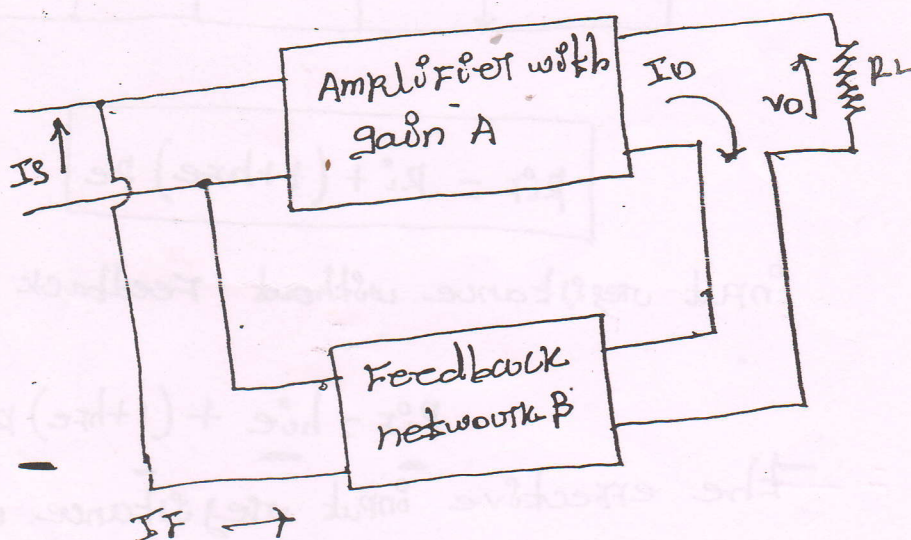
$$A_F = \frac{-h_{fe} R_L}{h_{ie} + (1+h_{fe}) R_e} \quad \text{--- (2)}$$

Output resistance ( $R_{oF}$ ) :-

$$R_{oF} = \frac{1+h_{fe}}{h_{oe}} = \frac{1}{h_{ob}} \quad \text{--- (3)}$$

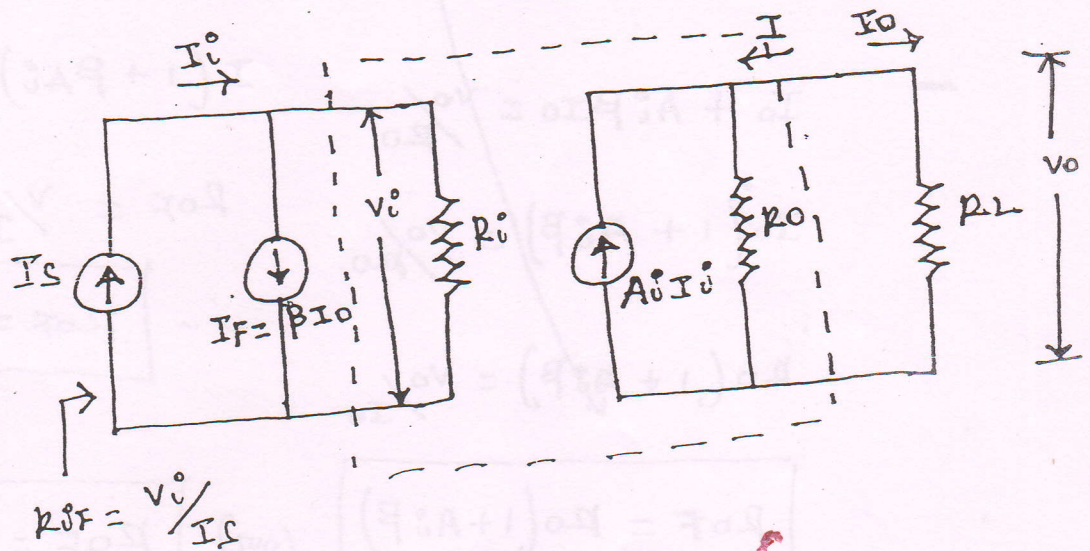
\* Current-Shunt Feedback :-

it is called a series-derived, shunt-fed Feedback. The shunt connection at the input reduces the input resistance and the series connection at the output increases the output resistance. The current feedback is given by  $\beta = I_F / I_O$





## Input and output resistance :-



Apply KCL to input side

$$I_s = I_i + I_F$$

$$I_s = I_i + \beta I_o$$

where  $I_o = A_v I_i$

$$\therefore I_s = I_i + A_v I_i \beta$$

$$I_s = I_i (1 + A_v \beta)$$

$$\therefore R_{iF} = v_o / I_s$$

$$\therefore I_o = v_o / r_o$$

$$R_{iF} = \frac{r_o}{(1 + A_v \beta)}$$

(out)

$$R_{oF} = \frac{r_o}{(1 + A_v \beta)}$$

Apply KCL to output side

$$I_o = v_o / r_o - A_v I_i$$

$$I = v_o / r_o - A_v I_i$$

$$\therefore (\text{where } -I_o = I)$$

$$I_i = -I_F = -\beta I_o$$

$$I_i = -I_F = -\beta I_o$$



$$\therefore I_o = \frac{V_o}{R_o} - A_i \beta I_o \quad I = \frac{V_o}{R_o} - \beta A_i I$$

$$I_o + A_i \beta I_o = \frac{V_o}{R_o}$$

$$I_o (1 + A_i \beta) = \frac{V_o}{R_o}$$

$$R_o (1 + A_i \beta) = \frac{V_o}{I_o}$$

$$R_{of} = R_o (1 + A_i \beta)$$

$$I (1 + \beta A_i) = \frac{V_o}{R_o}$$

$$R_{of} = \frac{V_o}{I}$$

$$\therefore R_{of} = R_o (1 + A_i \beta)$$

$$R_{of} = R_o (1 + A \beta)$$

Compare:- [6 mark]

| Characteristic      | Type of Feedback |                |            | G |
|---------------------|------------------|----------------|------------|---|
|                     | Current-Series   | Voltage-Series | Volt-Shunt |   |
| Voltage gain        | Decreases        | Decreases      | Decreases  |   |
| Bandwidth           | Increases        | Increases      | Increases  |   |
| Harmonic distortion | Decreases        | Decreases      | Decreases  |   |
| Noise               | Decreases        | Decreases      | Decreases  |   |
| Input resistance    | Increases        | Increases      | Decreases  |   |
| Output resistance   | Increases        | Decreases      | Decreases  |   |



## EFFECTS OF Negative Feedback:- [8mark]

- \* Improved stability of gain.
- \* Enhanced bandwidth.
- \* Decreased distortion
- \* Decreased noise
- \* Increase in input impedance
- \* Decrease in output impedance.

### \* Stabilization of Gain:-

The gain of the amplifier with Negative Feedback is  $A_F$

$$A_F = \frac{A}{1+AB}$$

Differentiating equation with respect to  $A$

$$\frac{dA_F}{dA} = \frac{1}{(1+AB)^2} = \frac{A_F}{A} \frac{1}{(1+AB)}$$

$$\frac{dA_F}{A_F} = \frac{dA}{A} \frac{1}{(1+AB)}$$

→ The term  $\frac{dA_F}{A_F}$  represents the fractional change in amplifier voltage gain with feedback.

→  $\frac{dA}{A}$  denotes the fractional change in voltage without feedback.



The sensitivity is defined as the ratio of Percentage change in voltage gain with Feedback to the Percentage change in voltage gain with Feedback.

$$\text{Sensitivity} = \frac{\left( \frac{dA_F}{A_F} \right)}{\left( \frac{dA}{A} \right)} = \frac{1}{(1+AB)}$$

The reciprocal of the term sensitivity is called desensitivity.

\* Increase of Bandwidth:-

The bandwidth of an amplifier is the difference between the upper cut off frequency  $F_2$  and lower cut off frequency  $F_1$ .

The Product of voltage gain and bandwidth of an amplifier without feedback and with feedback remains the same.

$$A_F \times B_{WF} = A \times BW$$

Due to the negative feedback in the amp the upper cut off frequency is increased by a factor  $(1+AB)$  and the lower cut off frequency  $F_{LF}$  is decreased by the same factor (it

$$F_{2F} = F_2 (1+AB) \text{ and } F_{1F} = \frac{F_1}{1+AB}$$



\* Decreased distortion:-

Consider an amplifier with an open loop voltage gain and a total harmonic distortion  $D$ . Then, with the introduction of Negative Feedback with the feedback ratio the distortion will reduce

$$D_F = \frac{D}{1+AB}$$

\* Decreased Noise:-

There are many sources of noise in an amplifier depending upon the active device used. With using the negative feedback with the feedback ratio,  $B$ , the noise  $N$ , be reduced by a factor  $1/(1+AB)$  in a similar manner to non-linear distortion.

$$N_F = \frac{N}{1+AB}$$

\* Increase in input impedance:-

The i/p impedance with feedback

is given

$Z_{iF} = Z_i(1+AB)$ . Thus the i/p impedance is increased by a factor of  $(1+AB)$ .

\* Decrease in output impedance:-

$$Z_{oF} = \frac{Z_o}{(1+AB)}$$

The output impedance is reduced by a factor  $(1+AB)$



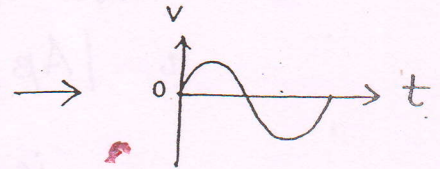
## Oscillators

A circuit which is used to generate a periodic voltage without an A.C. Input signal is called an oscillator.

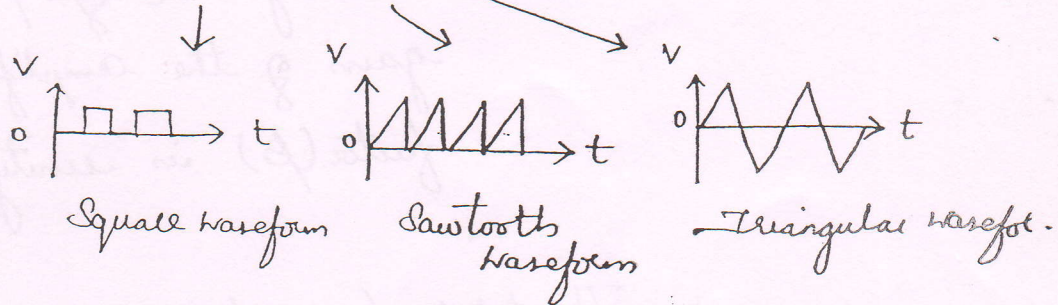
### Classification of Oscillators

#### 1. According to waveforms generated

1. Sinusoidal oscillator



2. Relaxation oscillator



#### 2. According to frequency generated

1. Audio frequency oscillator : upto  $20\text{kHz}$
2. Radio frequency oscillator :  $2\text{kHz}$  to  $30\text{MHz}$
3. Very high frequency oscillator :  $30\text{MHz}$  to  $300\text{MHz}$
4. Ultra high frequency oscillator :  $300\text{MHz}$  to  $3\text{GHz}$
5. Microwave frequency oscillator : above  $3\text{GHz}$ .

#### 3. According to fundamental mechanisms involved

1. Negative resistance oscillators
2. Feedback oscillators



4. According to type of circuit used
- 1. LC tuned oscillator  $\rightarrow$  Hartley, Colpitts, Clapp oscillator
  - 2. RC phase shift oscillator
  - 3. Wein bridge oscillator

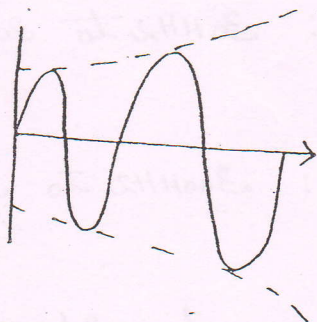
Conditions for oscillations (Barkhausen Criterion) \* 2 mark

1.  $|A\beta| = 1$

ie., The magnitude of product of the open loop gain of the amplifier (A) and the feedback factor ( $\beta$ ) is unity.

2. The total phase shift around the closed loop is Zero or 360 degrees.

(i)  $|A\beta| > 1$

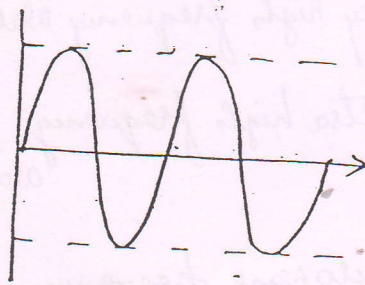


When total phase shift is  $0^\circ$  or  $360^\circ$

$|A\beta| > 1$ ,

oscillations produced are growing type oscillations

(ii)  $|A\beta| = 1$

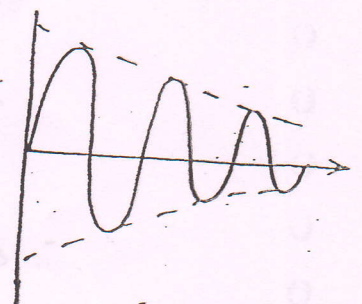


When total phase shift is  $0^\circ$  or  $360^\circ$

$|A\beta| = 1$ ,

oscillations produced are sustained oscillations

(iii)  $|A\beta| < 1$

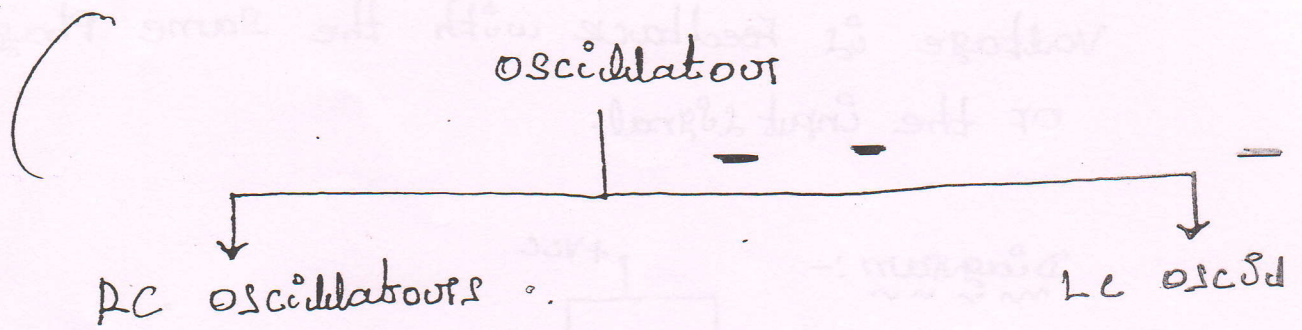


When total phase shift is  $0^\circ$  or  $360^\circ$

$|A\beta| < 1$ ,

oscillations produced are decaying type oscillations





- \* RC Phase shift oscillator
- \* Wein bridge oscillator

- \* Hartley os
- \* Colpitts osc
- \* Clapp osc

~~\* RC Phase shift oscillator :-~~

These oscillators employ inductors and capacitors and are used to generate ~~the~~ audio frequency signals. Hence they are known as audio frequency oscillators.

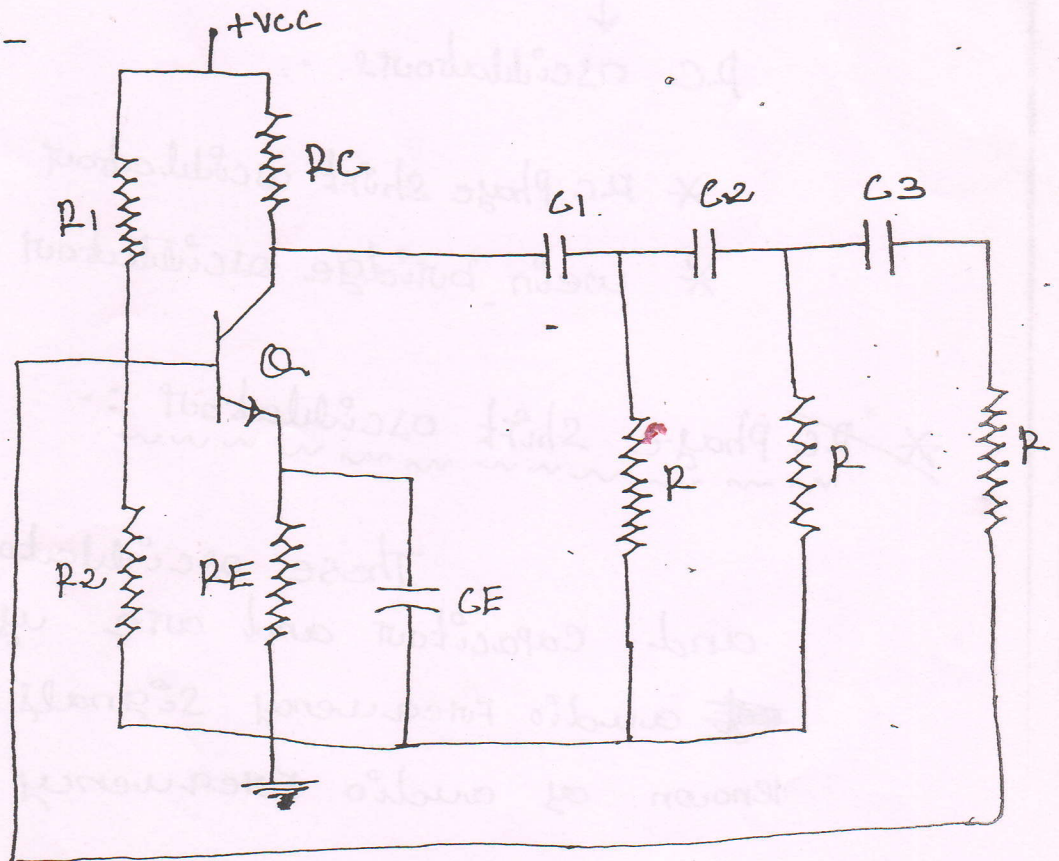
Basic Principle of RC oscillators :-

The common emitter amplifier only amplifies the input signal, but also introduces a phase shift of  $180^\circ$ . If we take a fraction of the output and feedback to the input, without considering the phase shift, the negative feedback takes place. Due to the negative feedback the output voltage of the amplifier decreases. However, for producing oscillations, we must have positive feedback of sufficient magnitude. This occurs only when the fraction of output



Voltage is feedback with the same phase as that of the input signal.

Diagram:-



The amplifier and feedback network is an  $-ve$ . The amplifier stage is self-biased with a capacitor by-passed emitter resistor ( $R_E$ ) and collector resistor ( $R_C$ ).

The feedback network consists of three identical RC sections. Each section produces a phase shift of  $60^\circ$ . Since the amplifier stage also introduces a phase shift of  $180^\circ$ , therefore the total phase shift between the input and output circuit is  $360^\circ$  or  $0^\circ$ .

When the circuit is energized by switching on the supply, the circuit starts oscillation.



The oscillation's may start due to the minor variation in dc supply. the variation in the base current is amplified in the collector circuit. then it's feedback through the phase shift network and finally applied to the ~~gate~~ base.

The oscillation will be maintained the loop gain ( $A_v B$ ) is at least equal to unity.

the circuit frequency is given

11

$$f_0 = \frac{1}{2\pi RC\sqrt{6+4k}} \quad \text{--- (1)}$$

the feedback fraction of RC phase shift network

$$B = \frac{1}{29} \quad \text{--- (2)}$$

using the value of  $B$  we find that for the loop gain ( $A_v B$ ) to be greater than unity. the gain of the amplifier stage must be greater than  $1/B$  or 29.

Advantages :-

- \* circuit is simple to design.
- \* produces sinusoidal output waveform.
- \* Fixed frequency oscillator.

Disadvantages :-

\* By changing the values of  $R$  &  $C$ , the frequency of oscillator can be changed.

\* Frequency stability is poor due to effect of temperature.

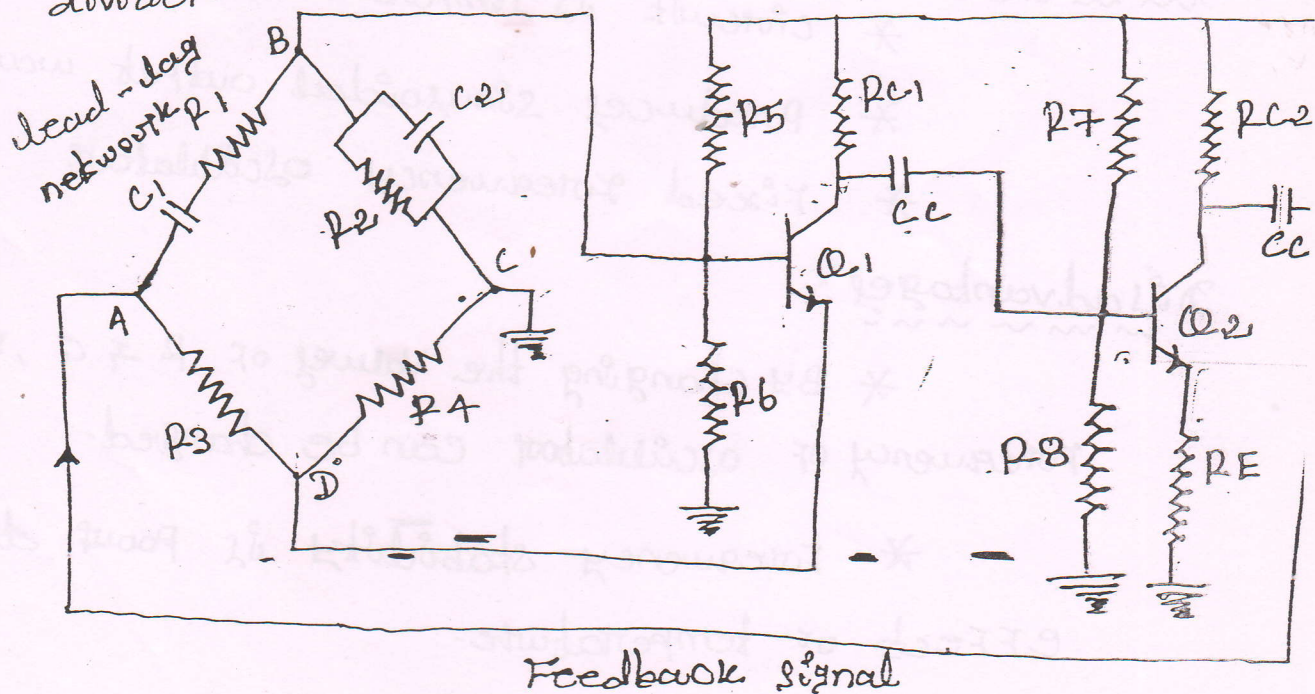


# \* Wein bridge oscillator :- [8 marks]

Phase shift oscillators have one drawback. i.e. when they are used to have a variable frequency circuit. it is difficult to adjust equally the capacitor values of the phase shift network simultaneously. An oscillator circuit which is more useful for variable frequency operation, is the wein bridge oscillator.

The wein bridge oscillator circuit consists of a two-stage RC coupled amplifier, which provides an approximately  $360^\circ$  or  $0^\circ$  phase shift. So, the feedback network has no need to introduce any additional phase-shift. The feedback network consists of  $C_1 - R_1$ ,  $C_2 - R_2$  (called a lead-lag network) and  $R_3 - R_4$  (called a voltage divider).

The lead-lag network provides a feedback to the input of the first stage and the voltage divider.





It can be shown by a simple analysis that the frequency of oscillation for the Wein bridge oscillator is given by the relation.

$$f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

$$\therefore R_1 = R_2 = R \\ C_1 = C_2 = C$$

$$f_0 = \frac{1}{2\pi RC}$$

When the circuit is energised by switching the supply. A small random oscillation appears at the base of  $Q_1$  transistor are amplified, at collector. These oscillations are further amplified at collector of  $Q_2$  transistor. Since the output at the collector of  $Q_2$  transistor have been in phase twice, therefore these oscillations are in phase with the input signal. A part of the output signal from the collector of  $Q_2$  transistor is feedback to the Wein-bridge, which is further amplified. The process continues, till sustained oscillations are produced.

The Wein bridge oscillator is a standard oscillator circuit for generating low frequencies in the range of 20 Hz to about 1 MHz.



Advantages :-

\* It gives an extremely pure sine wave output.

\* Good frequency stability.

\* highly stabilized amplitude.

\* Hartley oscillator :- [8 mark]

The tank circuit consists of two coils  $L_1$  and  $L_2$ . The coil  $L_1$  is inductively coupled to coil  $L_2$  and the combination works as an autotransformer. A coil called radio frequency choke (RFC) is connected between the collector and VCC supply.

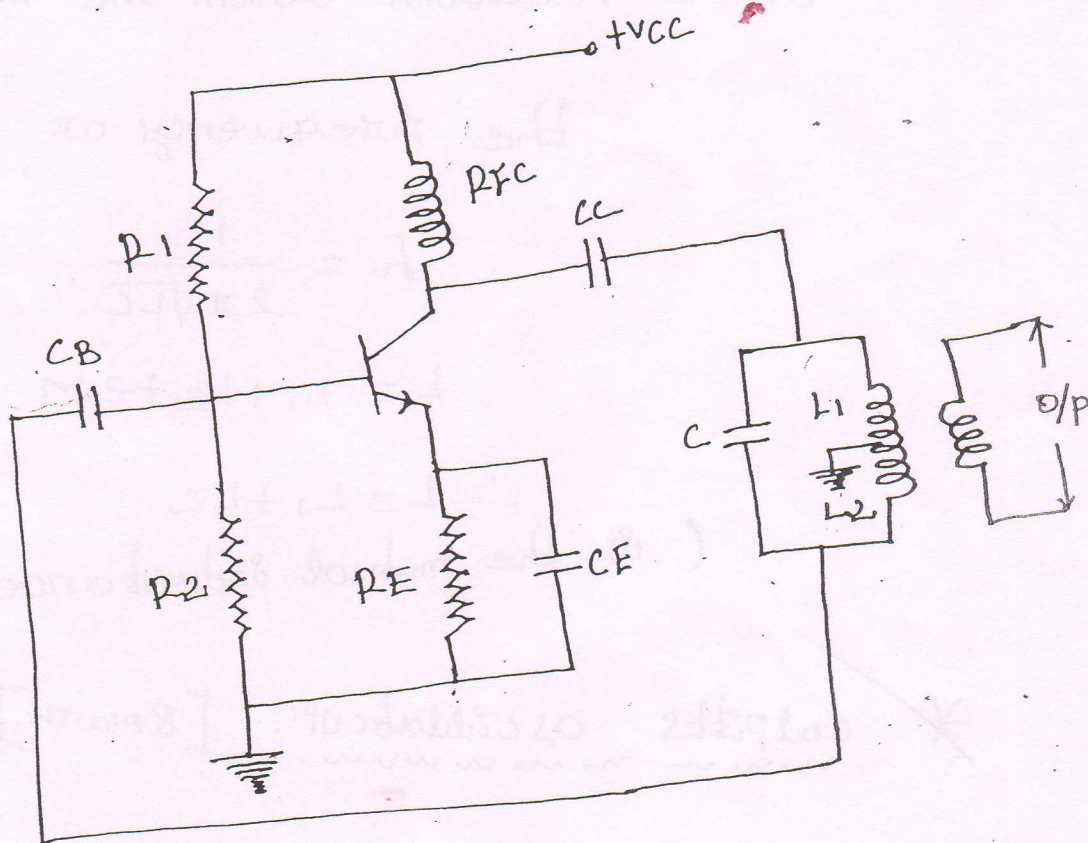
It acts as a load for the collector and also permits an easy flow of d.c current but blocks a.c.

The autotransformer ( $L_1$  and  $L_2$ ) introduces a phase shift of  $180^\circ$ . The phase reversal between the output and input voltages occurs because they are taken from the opposite ends of the coil with respect to the tap.



The  $L_1$  and  $L_2$  could actually be connected to the transistor emitter terminal via ground and through the capacitor (CE).

The transistor also introduces a phase shift, therefore the total phase shift  $360^\circ$  and hence the feedback is positive.



The capacitor  $C_C$ , connected between the collector and the tuned circuit, is called coupling capacitor.

It permits only the a.c. currents to pass to the tank circuit. The capacitor  $C_B$ , called blocking capacitor, further blocks the d.c. current.



The resistors  $R_1$ ,  $R_2$  and  $R_E$  are used to provide d.c bias to the transistor.

The circuit is energised, by switch on the supply, the collector current flows. The oscillations are produced because of positive feedback from the tank circuit.

The frequency of oscillation.

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

$$L = L_1 + L_2 + 2M$$

$$\therefore L \approx L_1 + L_2$$

(if the mutual inductance is neglected)

\* Colpitts Oscillator:- [8 marks]

The Colpitts oscillator uses tapped capacitance instead of tapped inductance as in Hartley oscillator. The tank circuit is made up of two capacitance  $C_1$  and  $C_2$  connected in series with each other across a fixed inductance.

The resistors ( $R_1$ ,  $R_2$  and  $R_E$ ), capacitors ( $C_C$  and  $C_B$ ) and  $R_{FC}$  have the function as



mentioned four hartley oscillators. The feedback between the output and input circuit is accomplished by the voltage developed across the capacitor  $C_2$ .

The feedback fraction

$$\beta = C_1/C_2$$

The frequency of oscillation is given by the equation.

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

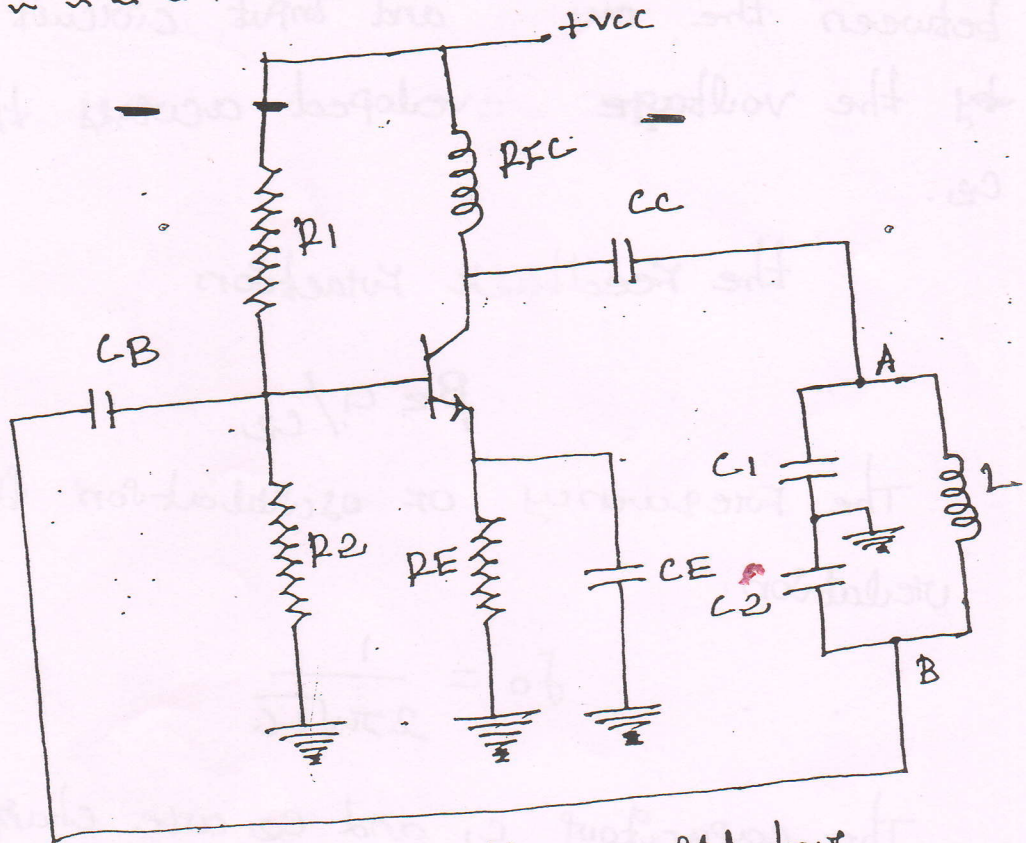
The capacitors  $C_1$  and  $C_2$  are charged. These capacitors discharge through the coil ( $L$ ), which sets up the oscillations of frequency  $f_0 = \frac{1}{2\pi\sqrt{LC}}$ .

The points A & B are  $180^\circ$  out of phase with each other. Another phase shift  $180^\circ$  is provided by the transistor itself. The total phase shift of  $360^\circ$  between the emitter-base and collector-base circuit.

The colpitts oscillators are widely used as a signal generator for frequency between 1 MHz and 500 MHz.



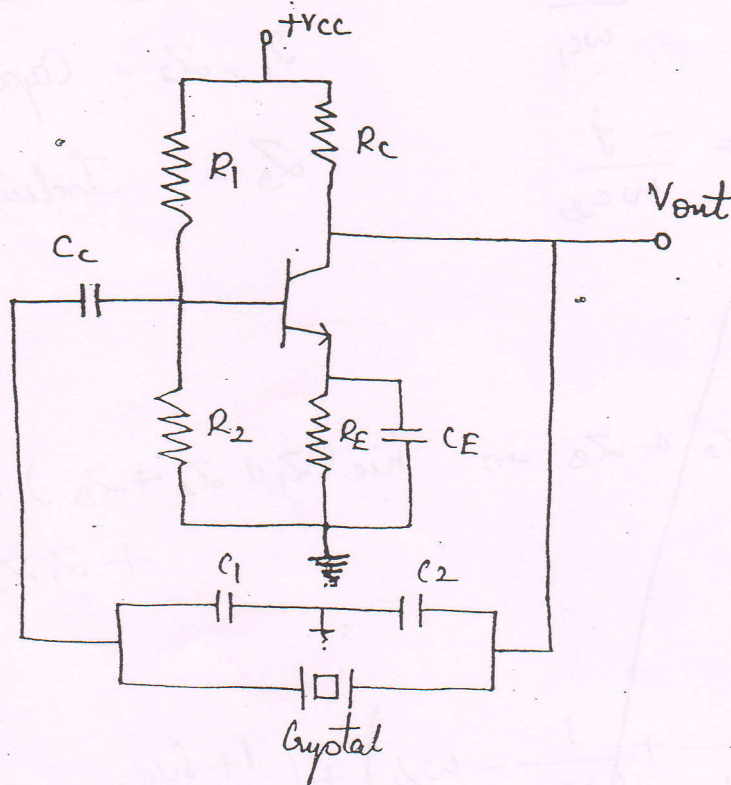
Circuit diagram:



Colpitts oscillator



## Crystal oscillator



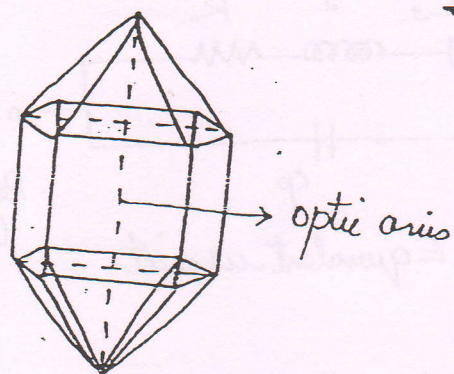
Colpitts crystal oscillator, in which the inductor is replaced by the crystal.

The crystal is a thin slice of piezo electric material, such as quartz, tourmaline & Rochelle salt which exhibits a property called Piezo-electric effect.

Piezo-electric effect represents the characteristics that the crystal reacts to any mechanical stress by producing an electric charge, in the reverse effect, an electric field results in mechanical strain.



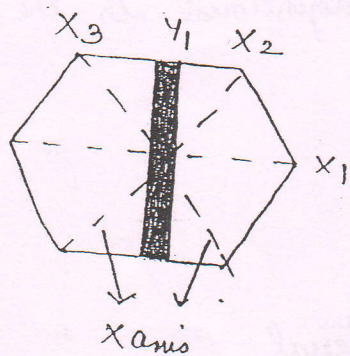
# Quartz crystal construction



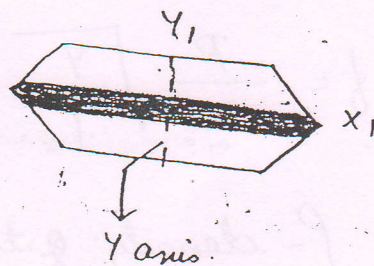
∴ To obtain high degree of frequency stability, crystal oscillators are used.

There are different methods of cutting the crystal wafer from crude quartz.

The method of cutting the crystal determines the natural resonant frequency + temperature Co-efficient of the crystal.



X-cut

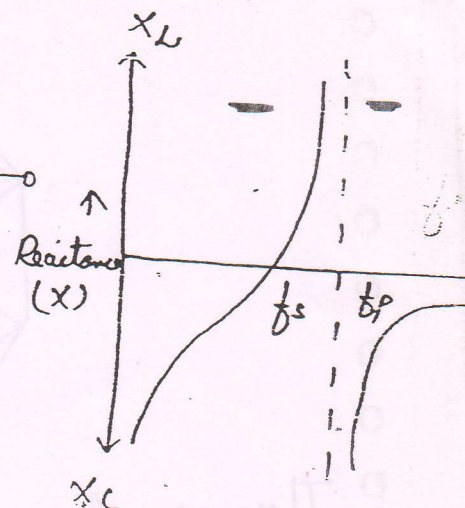
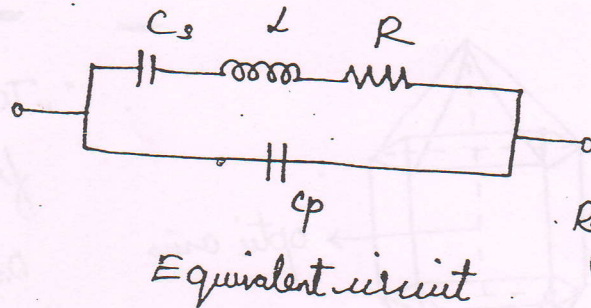
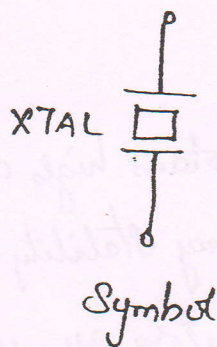


Y-cut

(i) When the wafer is cut in such a way that its flat surface are perpendicular to its electrical axis (X-axis), it is called an X-cut crystal.

(ii) When the wafer is cut in such a way that its flat surface are perpendicular to its mechanical axis (Y-axis), it is called an Y-cut crystal.





If an alternating voltage is applied, then the crystal wafers are set into vibration. The frequency of vibration equal to the resonant frequency of the crystal is determined by its structural characteristics.

Frequency of vibration is inversely proportional to the thickness of the crystal.

$$f = \frac{P}{2e} \sqrt{\frac{Y}{\rho}}$$

$\rho$  - density of the material.



47.

An Amplifier has an open loop gain of 1000 and a feedback of 0.04. If the open loop gain changes by 10% due to temperature, find the percentage change in gain of Amplifier with feedback.

$$A = 1000, \beta = 0.04 \quad \text{and} \quad \frac{dA}{A} = 10\%$$

$$\frac{dA_f}{A_f} = \frac{dA}{A} \cdot \frac{1}{1 + A\beta}$$

$$= 10 \cdot \frac{1}{1 + (1000)(0.04)}$$

$$\frac{dA_f}{A_f} = 0.25 \times 100$$

$$= 25\%$$

48

An Amplifier has Voltage gain with feedback of 100. If the gain without feedback changes by 20% and the gain with feedback should not vary more than 2%. Determine the values of open loop gain & feedback ratio  $\beta$ .

Given  $A_f = 100, \frac{dA_f}{A_f} = 2\% = 0.02 \quad \text{and} \quad \frac{dA}{A} = 20\% = 0.2$

$$\frac{dA_f}{A_f} = \frac{dA}{A} \cdot \frac{1}{1 + A\beta}$$

$$0.02 = 0.2 \times \frac{1}{1 + A\beta}$$

$$1 + A\beta = \frac{0.2}{0.02} = 10$$

Also gain with feedback is

$$A_f = \frac{A}{1 + A\beta}$$

$$100 = \frac{A}{10}$$

$$\boxed{A = 1000}$$

$$1 + A\beta = 10$$

$$1 + (1000)\beta = 10$$

$$\beta = \frac{9}{1000} = 0.009$$



49

An Amplifier has a midband gain of 125 & a bandwidth 250 KHz. (a) If 4% negative feedback is introduced, find new bandwidth & gain (b) If the bandwidth is to be restricted to 1 KHz, find the feedback ratio.

Given:  $A = 125$ ,  $B.W = 250 \text{ KHz}$  &  $\beta = 4\% = 0.04$

Solution

$$\begin{aligned} (a) \quad B.W_f &= (1 + A\beta) \cdot B.W \\ &= (1 + 125 \times 0.04) \times 250 \times 10^3 \\ B.W_f &= 1.5 \text{ KHz} \end{aligned}$$

Gain with feedback

$$A_f = \frac{A}{1 + A\beta}$$

$$A_f = \frac{125}{1 + 125 \times 0.04}$$

$$A_f = \frac{125}{6} = 20.83$$

$$(b) \quad B.W_f = (1 + A\beta) B.W$$

$$1 \times 10^6 = (1 + 125 \beta') \times 250 \times 10^3$$

$$1 + 125 \beta' = \frac{1 \times 10^6}{250 \times 10^3} = 4$$

$$\beta' = \frac{3}{125} = 0.024 = 2.4\%$$



50.

An Amplifier has a Voltage gain of 400,  $f_1 = 50\text{Hz}$ ,  $f_2 = 200\text{kHz}$  is a distortion of 10%. Without feedback. Determine the Amplifier Vol gain  $f_{1f}$ ,  $f_{2f}$  and  $D_f$  when a negative feedback is applied with feedback ratio of 0.01.

Given  $A = 400$ ,  $f_1 = 50\text{Hz}$ ,  $f_2 = 200\text{kHz}$ ,  $D = 10\%$  &  $\beta = 0.01$

Solution

$$A_f = \frac{A}{1 + A\beta}$$

$$A_f = \frac{400}{1 + 400 \times 0.01} = 80$$

New lower 3dB frequency

$$f_{1f} = \frac{f_1}{1 + A\beta} = \frac{50}{1 + 400 \times 0.01} = 10\text{Hz}$$

New upper 3dB frequency

$$f_{2f} = (1 + A\beta) \times f_2 = (1 + 400 \times 0.01) \times 200 \times 10^3 = 1\text{MHz}$$

Distortion with feedback

$$D_f = \frac{D}{1 + A\beta} = \frac{10}{5} = 2\%$$



51 \*

A Single Stage transistor amplifier has a Voltage of 600 with feedback & 50 with feedback. Calculate the percentage of output which is feedback to the Input.

Given  $A = 600$   
 $A_f = 50$

$$A_f = \frac{A}{1 + A\beta}$$

$$A_f = \frac{600}{1 + 600 \cdot \beta}$$

$$1 + 600\beta = \frac{600}{50}$$

$$1 + 600\beta = 12$$

$$600\beta = 11$$

$$\beta = 11/600 = 0.01833$$

$$\beta = 0.01833 \times 100$$

$$\boxed{\beta = 1.833}$$

521

A Voltage Series negative feedback Amplifier has a Voltage gain without feedback of  $A = 500$ .  $R_i = 3k\Omega$ ,  $R_o = 20k\Omega$ ,  $\beta = 0.01$ . Calculate the voltage gain  $A_f$ , Input resistance  $R_{if}$  & output resistance  $R_{of}$  of the Amplifier with feedback.

$$A_f = \frac{A}{1 + A\beta} = \frac{500}{1 + 500 \times 0.01} = \frac{500}{6} = 83.33$$

$$R_{if} = (1 + A\beta) R_i$$

$$= (1 + 500 \times 0.01) \times 3 \times 10^3 = 18k\Omega$$



$$R_{of} = \frac{R_o}{1+A\beta} = \frac{20 \times 10^3}{1+500 \times 0.01}$$

$$R_{of} = 3.3k\Omega$$

53.

In Hartley oscillator  $L_2 = 0.4mH$  &  $C = 0.004\mu F$ . If the frequency of the oscillator is  $120kHz$ . find the value of  $L_1$ .

Neglect the mutual Inductance.

$$f_o = \frac{1}{2\pi \sqrt{(L_1 + L_2) C}}$$

$$(L_1 + L_2) C = \frac{1}{4\pi^2 f_o^2}$$

$$L_1 = \frac{1}{4\pi^2 f_o^2 \cdot C} - L_2$$

$$L_1 = \frac{1}{4\pi^2 (120 \times 10^3)^2 \times 0.004 \times 10^{-6}} - 0.4 \times 10^{-3}$$

$$L_1 = 0.44 \times 10^{-3} - 0.4 \times 10^{-3}$$

$$L_1 = 0.04mH$$

54.

In a transistorized Hartley Oscillator the two inductances  $2mH$  and  $20\mu H$  while the frequency is to be changed from  $950kHz$  to  $2050kHz$ . calculate the range over which the capacitor is to be varied

$$f_o = \frac{1}{2\pi \sqrt{(L_1 + L_2) C}}$$



$$C = \frac{1}{4\pi^2 (\alpha_1 + \alpha_2) f_0^2}$$

$$\text{then } f_0 = 950 \text{ kHz}$$

$$C = \frac{1}{4\pi^2 [(2 \times 10^{-3} + 20 \times 10^{-6}) (950 \times 10^3)^2]}$$

$$C = 13.89 \text{ pF}$$

$$\text{then } f_0 = 2050 \text{ kHz}$$

$$C = \frac{1}{4\pi^2 [(2 \times 10^{-3} + 20 \times 10^{-6}) (2050 \times 10^3)^2]}$$

$$C = 2.98 \text{ pF}$$

55.

In a hartley oscillator, the value of the capacitor in the tuned circuit is  $500 \text{ pF}$  & the two sections of coils have inductances  $38 \mu\text{H}$  &  $12 \mu\text{H}$ . Find the frequency of oscillations & the feedback factor  $\beta$ .

$$f_0 = \frac{1}{2\pi \sqrt{LC}}$$

$$\begin{aligned} L &= L_1 + L_2 = 38 \times 10^{-6} + 12 \times 10^{-6} \\ &= 50 \times 10^{-6} = 50 \mu\text{H} \end{aligned}$$

$$C = 500 \text{ pF}$$

$$f_0 = \frac{1}{2\pi \sqrt{50 \times 10^{-6} \times 500 \times 10^{-12}}}$$

$$f_0 = 1 \text{ MHz}$$

$$\beta = \frac{L_1}{L_2} = \frac{38 \times 10^{-6}}{12 \times 10^{-6}} = 3.166$$



## Wein Bridge Oscillator:

### Derivation of Frequency:

The feedback Network of Wein bridge oscillator is shown. It consists of two arm  $R_1, C_1$  in series and  $R_2, C_2$  are in parallel it is called frequency sensitive arm.

Input to feedback network is  $V_{in}$  and output of feedback network is  $V_f$ .

From the fig we can write

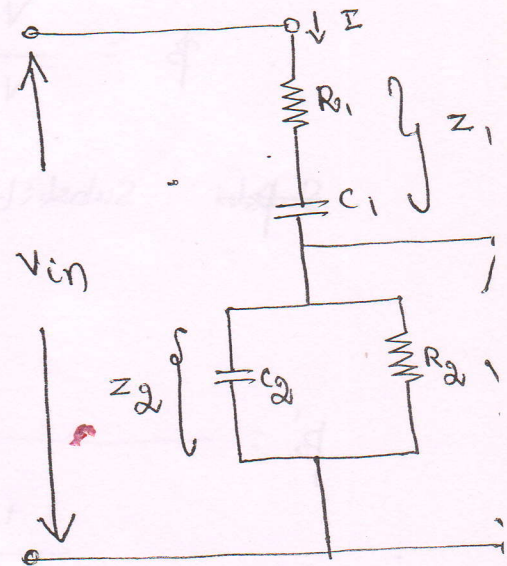


Fig. Feedback network of Wein bridge oscillator

$$Z_1 = R_1 + \frac{1}{j\omega C_1} = \frac{j\omega C_1 R_1 + 1}{j\omega C_1} \quad \text{--- (1)}$$

$$Z_2 = R_2 \parallel \frac{1}{j\omega C_2} = \frac{R_2 \times \frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}} = \frac{\cancel{R_2} / j\omega C_2}{(j\omega C_2 R_2 + 1) / j\omega C_2}$$

$$Z_2 = \frac{R_2}{(j\omega C_2 R_2 + 1)} \quad \text{--- (2)}$$

Current through the circuit can be written as

$$I = \frac{V_{in}}{Z_1 + Z_2} \quad \text{--- (3)}$$

Similarly voltage across  $Z_2$  can be written as

$$V_f = I Z_2 \quad \text{--- (4)}$$

Substitute equ (3) in (4) we get.



$$V_f = \frac{Z_2}{(Z_1 + Z_2)} V_{in} \Rightarrow \frac{V_f}{V_{in}} = \frac{Z_2}{Z_1 + Z_2}$$

$$\beta = \frac{V_f}{V_{in}} = \frac{Z_2}{Z_1 + Z_2} \dots \dots (5)$$

~~Subst~~ Substitute equ (1) & (2) in (5) we get

$$\beta = \frac{\frac{R_2}{1 + j\omega R_2 C_2}}{\frac{1 + j\omega R_1 C_1}{j\omega C_1} + \frac{R_2}{1 + j\omega R_2 C_2}}$$

$$= \frac{R_2 / (1 + j\omega R_2 C_2)}{(1 + j\omega R_1 C_1)(1 + j\omega R_2 C_2) + j\omega C_1 R_2}$$

$$= \frac{j\omega R_2 C_1}{(1 + j\omega R_1 C_1)(1 + j\omega R_2 C_2) + j\omega C_1 R_2}$$

$$= \frac{j\omega R_2 C_1}{1 + j\omega R_2 C_2 + j\omega R_1 C_1 - \omega^2 R_1 C_1 R_2 C_2 + j\omega C_1 R_2}$$

$$\beta = \frac{j\omega R_2 C_1}{(1 - \omega^2 R_1 C_1 R_2 C_2) + j\omega [R_2 C_2 + R_1 C_1 + C_1 R_2]} \quad \dots (6)$$



Now multiply numerator and denominator by  $(1 - \omega^2 R_1 R_2 C_1 C_2) - j\omega (R_1 C_1 + R_2 C_2 + R_2 C_1)$  to eqn (8)

$$\beta = \frac{j\omega R_2 C_1 [(1 - \omega^2 R_1 R_2 C_1 C_2) - j\omega (R_1 C_1 + R_2 C_2 + R_2 C_1)]}{(1 - \omega^2 R_1 R_2 C_1 C_2)^2 + \omega^2 [R_1 C_1 + R_2 C_2 + R_2 C_1]^2}$$

$$\beta = \frac{j\omega R_2 C_1 - j\omega^3 R_1 R_2 C_1 C_2 + \omega^2 R_2 C_1 (R_1 C_1 + R_2 C_2 + R_2 C_1)}{(1 - \omega^2 R_1 R_2 C_1 C_2)^2 + \omega^2 [R_1 C_1 + R_2 C_2 + R_2 C_1]^2}$$

In order to have zero phase shift imaginary part of above equation become zero.

$$\therefore \frac{\omega R_2 C_1 (1 - \omega^2 R_1 R_2 C_1 C_2)}{[1 - \omega^2 R_1 R_2 C_1 C_2]^2 + \omega^2 [R_1 C_1 + R_2 C_2 + R_2 C_1]^2} = 0$$

$$(1 - \omega^2 R_1 R_2 C_1 C_2) = 0$$

$$\omega^2 R_1 R_2 C_1 C_2 = 1$$

$$\omega^2 = \frac{1}{R_1 R_2 C_1 C_2}$$

$$2\pi f = \omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$f = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}} \quad \text{--- (8)}$$

In practice  $R_1 = R_2 = R$  and  $C_1 = C_2 = C$

$$\therefore f = \frac{1}{2\pi RC} \quad \text{--- (9)}$$



using  $\omega = \frac{1}{R_C C}$  in (7) we get.

$$\beta = \frac{1}{3}$$

Substitute  $\beta$  value in Barkhausen criterion we

get.  $|A\beta| \geq 1$

$$|A \cdot \frac{1}{3}| \geq 1$$

$$\therefore |A| \geq 3 \text{ for Wein bridge oscillator}$$

Therefore the gain of an amplifier stage must be at least 3 to ensure sustained oscillation in Wein bridge Oscillator.

X ————— X

### Hartley Oscillator:-

#### Derivation of frequency of oscillations:-

The output current is collector current which is  $h_{fe} I_B$ , where  $I_B$  is base current. As emitter is grounded for a.c. analysis,  $L_1$  is between emitter and base while  $L_2$  is between emitter and collector. and its equivalent circuit is shown.

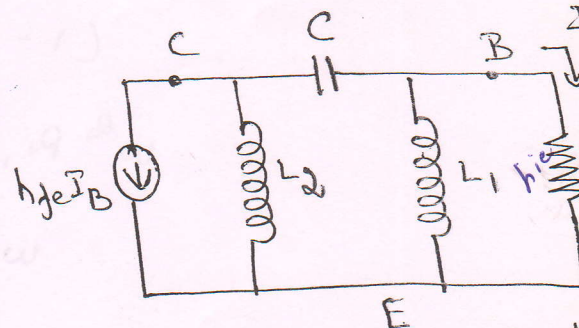


Fig. Equivalent circuit

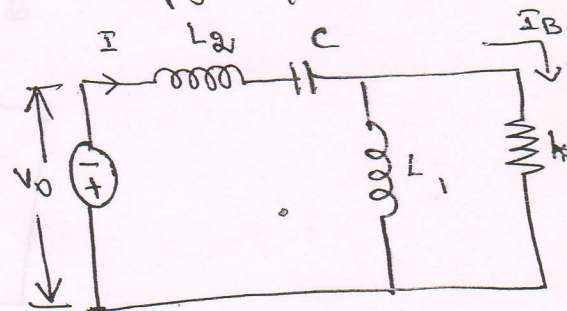


Fig. Simplified equivalent circuit

Now convert the current source to voltage source and it is shown in this fig.



From the simplified equivalent circuit we can

write  $V_o = h_f \bar{I}_B X_{L2} = h_f \bar{I}_B j\omega L_2 \quad \dots (1)$

The total current  $\bar{I}$  can be written as

$$\bar{I} = \frac{-V_o}{[X_{L2} + X_C] + [X_{L1} || h_{ie}]} \quad \dots (2)$$

The negative sign in above equation is due to direction of  $\bar{I}$  is opposite to polarities of  $V_o$ .

we know that

$$X_{L2} + X_C = j\omega L_2 + \frac{1}{j\omega C} = \frac{-\omega^2 L_2 C + 1}{j\omega C} \quad \dots (3)$$

$$X_{L1} || h_{ie} = \frac{j\omega L_1 \times h_{ie}}{j\omega L_1 + h_{ie}} \quad \dots (4)$$

Now substitute (1), (3) & (4) in equ (2) we get.

$$\bar{I} = \frac{-h_f \bar{I}_B j\omega L_2}{\left[ \frac{1 - \omega^2 L_2 C}{j\omega C} \right] + \left[ \frac{j\omega L_1 h_{ie}}{j\omega L_1 + h_{ie}} \right]} \quad \dots (5)$$

Using current dividing rule in parallel combination.

$$\bar{I}_B = \left[ \frac{j\omega L_1}{j\omega L_1 + h_{ie}} \right] \bar{I} \quad \dots (6)$$

Substitute equ (5) in (6) we get.

$$\bar{I}_B = \frac{j\omega L_1}{(j\omega L_1 + h_{ie})} \times \frac{-h_f \bar{I}_B j\omega L_2}{\left[ \frac{1 - \omega^2 L_2 C}{j\omega C} \right] + \left[ \frac{j\omega L_1 h_{ie}}{j\omega L_1 + h_{ie}} \right]} \quad \dots (7)$$



$$\frac{I_B}{I} = \frac{w^2 L_1 L_2 h_{ie} \cancel{I_B}}{\left[ \frac{[1 - w^2 C L_2] (jw L_1 + h_{ie}) + [jw L_1 h_{ie}] jw C}{jw C [jw L_1 + h_{ie}]} \right] (jw L_1 + h_{ie})}$$

$$1 = \frac{w^2 L_1 L_2 h_{ie}}{\left( \frac{jw L_1 + h_{ie} - jw^3 C L_2 L_1 - w^2 C L_2 h_{ie} - w^2 L_1 h_{ie}}{jw C} \right)}$$

$$1 = \frac{w^2 L_1 L_2 h_{ie} (jw C)}{jw L_1 + h_{ie} - jw^3 C L_1 L_2 - w^2 C h_{ie} [L_2 + L_1]}$$

$$1 = \frac{jw^3 L_1 L_2 h_{ie} C}{[h_{ie} - w^2 C h_{ie} (L_1 + L_2)] + jw L_1 [1 - w^2 C L_2]} \quad (8)$$

Now multiply numerator and denominator by  $[h_{ie} - w^2 C h_{ie} (L_1 + L_2)] - jw L_1 [1 - w^2 C L_2]$  we get.

$$1 = \frac{jw^3 L_1 L_2 h_{ie} C \left\{ [h_{ie} - w^2 C h_{ie} (L_1 + L_2)] - jw L_1 [1 - w^2 C L_2] \right\}}{[h_{ie} - w^2 C h_{ie} (L_1 + L_2)]^2 + w^2 L_1^2 [1 - w^2 C L_2]^2 + \left( jw^3 L_1 L_2 h_{ie} C h_{ie} - jw^5 h_{ie} h_{ie} C L_1 L_2 (L_1 + L_2) + w^4 L_1^2 L_2 h_{ie} C [1 - w^2 C L_2] \right)}$$



$$1 = \frac{\omega^4 L_1^2 L_2 h j e C (1 - \omega^2 C L_2) + j \left[ \frac{\omega^3 L_1 L_2 h j e C h i e}{\omega^5 h j e h i e C^2 L_1 L_2 (L_1 + L_2)} - \right]}{\left[ h i e - \omega^2 C h i e (L_1 + L_2) \right]^2 + \omega^2 L_1^2 \left[ 1 - \omega^2 C L_2 \right]^2}$$

To have zero phase shift imaginary part of above equation must be zero.

$$\therefore \frac{\left[ \omega^3 L_1 L_2 h j e C h i e - \omega^5 h j e h i e C^2 L_1 L_2 (L_1 + L_2) \right]}{\left[ h i e - \omega^2 C h i e (L_1 + L_2) \right]^2 + \omega^2 L_1^2 (1 - \omega^2 C L_2)^2} = 0$$

$$\omega^3 L_1 L_2 h j e C h i e = \omega^5 h j e h i e C^2 L_1 L_2 (L_1 + L_2)$$

$$\omega^2 = \frac{1}{C (L_1 + L_2)}$$

taking square root on both side we get.

$$\omega = 2\pi f = \frac{1}{\sqrt{C (L_1 + L_2)}}$$

$$f = \frac{1}{2\pi \sqrt{C (L_1 + L_2)}}$$

(10)

Practically  $L_1$  and  $L_2$  are wound on a single core and there exist a mutual inductance  $M$  between them.

$$L = L_1 + L_2 + 2M$$

∴ Mutual inductance is neglected.

$$L = L_1 + L_2$$

(11)

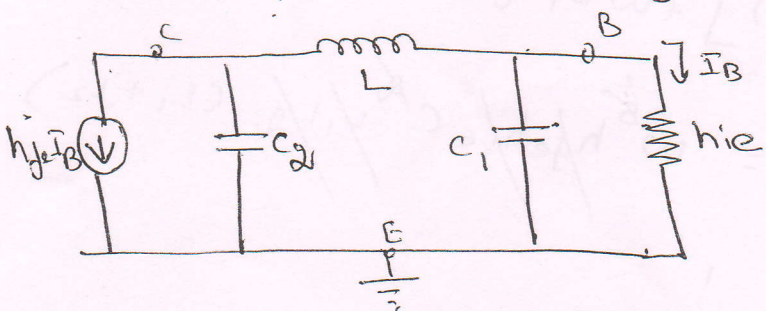


Substitute equ (11) in (10) we get,

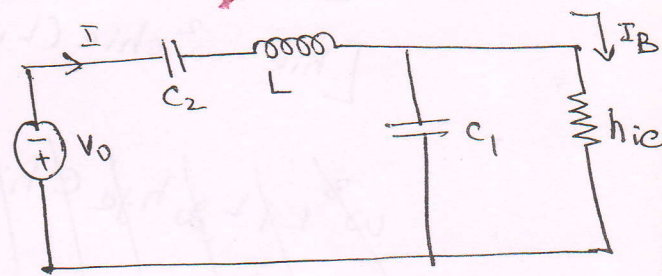
$$f = \frac{1}{2\pi \sqrt{L_{eq} C}} \quad \text{--- (12)}$$

## Colpitts Oscillator:-

Derivation of frequency of oscillation:-



(a) Equivalent circuit



(b) Simplified equivalent circuit

From the above simplified equivalent circuit we

can write

$$V_O = + h_{ie} I_B \times C_2 = \frac{h_{ie} I_B}{j\omega C_2} = \frac{-j h_{ie} I_B}{\omega C_2}$$

$$\therefore V_O = \frac{-j h_{ie} I_B}{\omega C_2} \quad \text{--- (1)}$$

The total current "I" can be written as

$$I = \frac{-V_O}{[X_{C2} + X_L] + [X_{C1} || h_{ie}]} \quad \text{--- (2)}$$

The negative sign in above equation is due to direction of I is opposite to polarities of  $V_O$ .



where as we know that

$$X_{C2} + X_L = \frac{1}{j\omega C_2} + j\omega L = \frac{-j}{\omega C_2} + j\omega L = \frac{-j + j\omega^2 L C_2}{\omega C_2}$$

$$\therefore X_{C2} + X_L = \frac{-j(1 - \omega^2 L C_2)}{\omega C_2} \quad \text{--- (2)}$$

$$X_{C1} I_{hie} = \frac{\frac{1}{j\omega C_1} \times h_{ie}}{\frac{1}{j\omega C_1} + h_{ie}} = \frac{\frac{-j}{\omega C_1} \times h_{ie}}{\frac{-j}{\omega C_1} + h_{ie}} = \frac{\frac{-j h_{ie}}{\omega C_1}}{\frac{-j + h_{ie} \omega C_1}{\omega C_1}}$$

$$\therefore X_{C1} I_{hie} = \frac{-j h_{ie}}{-j + h_{ie} \omega C_1} \quad \text{--- (4)}$$

Now substitute equ (1), (3) and (4) in equ (2) we get

$$I = \frac{- \left[ \frac{-j h_{ie} I_B}{\omega C_2} \right]}{\frac{-j(1 - \omega^2 L C_2)}{\omega C_2} + \left( \frac{-j h_{ie}}{-j + h_{ie} \omega C_1} \right)} \quad \text{--- (5)}$$

Apply Current dividing rule to simplified equivalent circuit parallel elements we can write

$$I_B = \frac{\frac{-j}{\omega C_1}}{\frac{-j}{\omega C_1} + h_{ie}} (I) = \frac{-j I}{-j + \omega C_1 h_{ie}} \quad \text{--- (6)}$$

Now substitute equ (5) in equ (6) we get



$$\bar{I}_B = \frac{-j}{-j + \omega C_1 h_{ie}} \times \frac{- \left( \frac{-j h_{fe} \bar{I}_B}{\omega C_2} \right)}{\frac{-j(1 - \omega^2 L C_2)}{\omega C_2} + \left( \frac{-j h_{ie}}{-j + \omega C_1 h_{ie}} \right)}$$

$$= \frac{\cancel{\omega C_2} \cdot h_{fe} \bar{I}_B}{(-j + \cancel{\omega C_1 h_{ie}}) \left[ \frac{-j(1 - \omega^2 L C_2)(-j + \omega C_1 h_{ie}) - j h_{ie} \omega C_2}{\cancel{\omega C_2} (-j + \cancel{\omega C_1 h_{ie}})} \right]}$$

$$h_{fe} \bar{I}_B$$

$$\bar{I}_B = \frac{h_{fe} \bar{I}_B}{\left[ (-j + j \omega^2 L C_2)(-j + \omega C_1 h_{ie}) - j h_{ie} \omega C_2 \right]}$$

$$h_{fe} \bar{I}_B$$

$$= \frac{h_{fe} \bar{I}_B}{\left[ -1 - j \omega C_1 h_{ie} + \omega^2 L C_2 + j \omega^3 L C_1 C_2 h_{ie} - j h_{ie} \omega C_2 \right]}$$

$$h_{fe} \bar{I}_B$$

$$\bar{I}_B = \frac{h_{fe} \bar{I}_B}{\left[ (-1 + \omega^2 L C_2) - j \omega h_{ie} \left[ C_1 + L C_1 C_2 \omega^2 + C_2 \right] \right]}$$

$$- \quad h_{fe} \bar{I}_B$$

$$\cancel{\bar{I}_B} = \frac{\cancel{h_{fe} \bar{I}_B}}{\left[ (1 - \omega^2 L C_2) + j \omega h_{ie} (C_1 + C_2 - \omega^2 L C_1 C_2) \right]}$$



$$1 = \frac{-hye}{(1 - \omega^2 L C_2) - j\omega L C_1 [C_1 + C_2 - \omega^2 L C_1 C_2]} \quad \dots (7)$$

In order to have zero phase shift imaginary part of above equation become zero.

$$\therefore \text{while } [C_1 + C_2 - \omega^2 L C_1 C_2] = 0 \quad \dots (8)$$

$$C_1 + C_2 - \omega^2 L C_1 C_2 = 0$$

$$C_1 + C_2 = \omega^2 L C_1 C_2$$

$$\omega^2 = \frac{C_1 + C_2}{L C_1 C_2} = \frac{1}{L \left[ \frac{C_1 C_2}{C_1 + C_2} \right]}$$

$$\omega^2 = \frac{1}{L C_{eqn}}$$

$$\text{where } C_{eqn} = \frac{C_1 C_2}{C_1 + C_2}$$

Taking root on both side we get.

$$\omega = \frac{1}{\sqrt{L C_{eqn}}}$$

$$\therefore 2\pi f = \frac{1}{\sqrt{L C_{eqn}}}$$

$$f = \frac{1}{2\pi \sqrt{L C_{eqn}}} \quad \dots (9)$$

The above equation represent the frequency of oscillation of Colpitts Oscillator.



## RC Phase Shift Oscillator:

### Derivation for frequency of Oscillation:

Draw the h-parameter equivalent circuit for RC phase shift oscillator. Then the equivalent circuit diagram for RC phase shift oscillator is

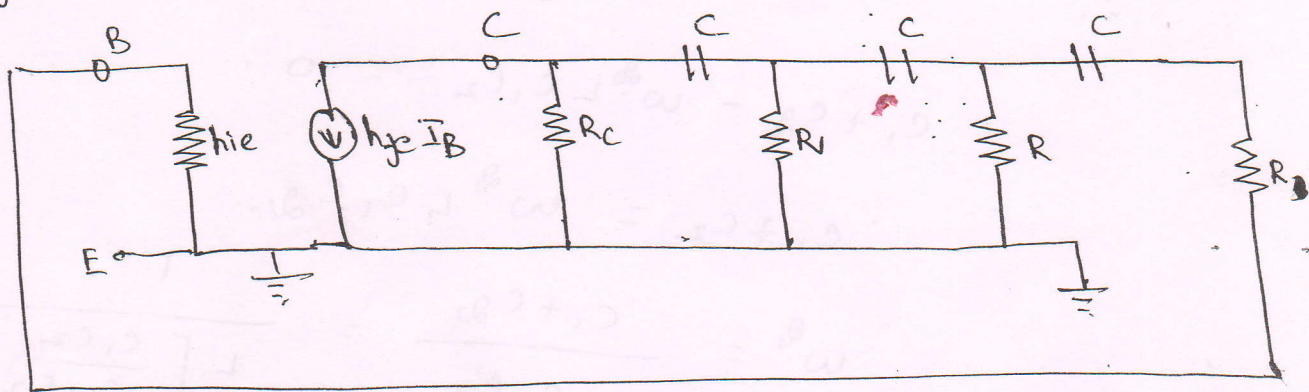


Fig. Equivalent circuit using h-parameter model.

Now replace the current source by equivalent voltage source then the above circuit can be redrawn as

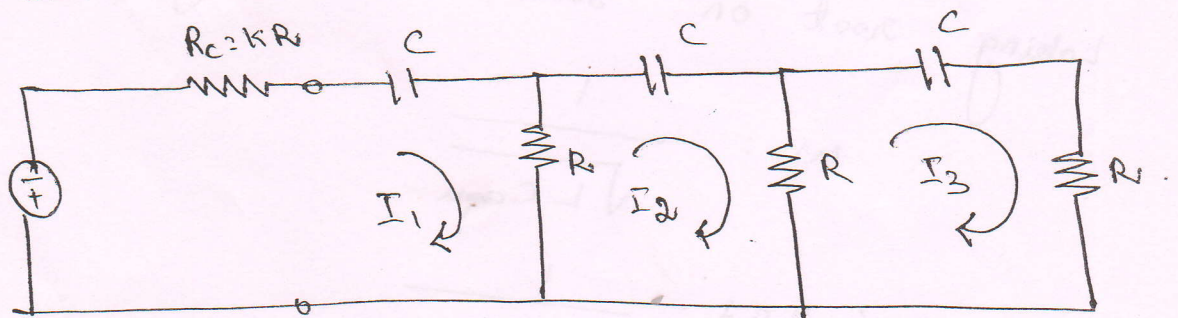


Fig. Modified equivalent circuit.

The ratio of resistance  $R_c$  to  $R$  is  $K$ .

$$\therefore K = \frac{R_c}{R}$$

Now apply KVL to the three loops in above circuit diagram, we get



For 1<sup>st</sup> loop:

$$-I_1 R_c - \frac{1}{j\omega C} I_1 - R(I_1 - I_2) - h_{fe} I_B R_c = 0$$

Substitute  $R_c = KR$  in above expression

$$-I_1 KR - \frac{1}{j\omega C} I_1 - R I_1 + R I_2 - h_{fe} I_B R_c = 0$$

$$-I_1 \left[ KR + \frac{1}{j\omega C} + R \right] + I_2 R = h_{fe} I_B R_c \quad \dots (1)$$

For 2<sup>nd</sup> loop:

$$-\frac{1}{j\omega C} I_2 - R(I_2 - I_1) - R(I_2 - I_3) = 0$$

$$-\frac{1}{j\omega C} I_2 - R I_2 + R I_1 - R I_2 + R I_3 = 0$$

$$R I_1 - I_2 \left[ \frac{1}{j\omega C} + 2R \right] + R I_3 = 0 \quad \dots (2)$$

For 3<sup>rd</sup> loop:

$$-\frac{1}{j\omega C} I_3 - I_3 R - R(I_3 - I_2) = 0$$

$$-\frac{1}{j\omega C} I_3 - I_3 R - I_3 R + I_2 R = 0$$

$$+ I_2 R - I_3 \left[ \frac{1}{j\omega C} + 2R \right] = 0 \quad \dots (3)$$

Assign  $j\omega = s$  and using Cramer's rule we can write

$$D = \begin{vmatrix} -(1+K)R - \frac{1}{sC} & R & 0 \\ R & -2R - \frac{1}{sC} & R \\ 0 & R & -2R - \frac{1}{sC} \end{vmatrix}$$

(using expression 1, 2 and 3)

--- (4)



Solving the determinant in (4) we get.

$$D = - \frac{s^3 R^3 (3K+1) + s^2 C^2 R^2 (4K+6) + sCR (5+K) + 1}{s^3 C^3}$$

Similarly Consider eqn (1), (2) and (3) and solve for  $D_3$  we write in matrix form.

$$D_3 = \begin{vmatrix} -(1+K)R - \frac{1}{sC} & R & h_{fe} I_B K R \\ R & -2R - \frac{1}{sC} & 0 \\ 0 & R & 0 \end{vmatrix} \quad \dots (6)$$

By solving the above determinant we get.

$$D_3 = K R^3 h_{fe} I_B \quad \dots (7)$$

$\therefore$  Output current of the feedback circuit  $I_3$  can be written as

$$I_3 = \frac{D_3}{D} = \frac{-K R^3 h_{fe} I_B s^3 C^3}{s^3 C^3 R^3 (3K+1) + s^2 C^2 R^2 (4K+6) + sCR (5+K) + 1}$$

$I_C = h_{fe} I_B$  (Input current to feedback circuit).

$$\therefore \beta = \frac{\text{Output of feedback circuit}}{\text{Input to feedback circuit}} = \frac{I_3}{I_C} = \frac{I_3}{h_{fe} I_B} \quad \dots (8)$$

$$A = \frac{\text{Output of the amplifier}}{\text{Input to the amplifier}} = \frac{I_3}{I_B} = h_{fe} \quad \dots (10)$$



$$A\beta = \cancel{h_{fe}} \times \frac{I_3}{\cancel{h_{fe} I_B}} = \frac{I_3}{I_B} \quad \text{--- (11)}$$

Now substitute equ (8) in (11) we get.

$$A\beta = \frac{-KR^3 h_{fe} \cancel{I_B} s^3 c^3}{[s^3 c^3 R^3 (3k+1) + s^2 c^2 R^2 (4k+6) + sRC(5+k) + 1] \cancel{I_B}} \quad \text{--- (12)}$$

Now replace s by jw we get.

$$A\beta = \frac{-KR^3 h_{fe} (-j\omega^3) c^3}{[-j\omega^3 c^3 R^3 (3k+1) + (-\omega^2) c^2 R^2 (4k+6) + j\omega RC(5+k) + 1]}$$

$$= \frac{j\omega^3 k R^3 c^3 h_{fe}}{[1 - \omega^2 c^2 R^2 (4k+6)] - j\omega [3k\omega^2 c^3 R^3 + \omega^2 c^2 R^2 (5+k)]}$$

$$A\beta = \frac{j\omega^3 k R^3 c^3 h_{fe}}{[1 - \omega^2 c^2 R^2 (4k) - 6\omega^2 c^2 R^2] - j\omega [3k\omega^2 c^3 R^3 + \omega^2 c^2 R^2 (5+k)]}$$

Now dividing numerator and denominator by  $j\omega^3 R^3 c^3$  and replace  $\frac{-1}{j} = j$  then equ (13) can be written as

$$A\beta = \frac{j\omega^3 k R^3 c^3 h_{fe} / j\omega^3 R^3 c^3}{[1 - \omega^2 c^2 R^2 (4k) - 6\omega^2 c^2 R^2] - j\omega [3k\omega^2 c^3 R^3 + \omega^2 c^2 R^2 (5+k)]}$$



Khje

$$A\beta = \frac{\left[ \frac{1}{j\omega^3 R^3 C^3} - \frac{4k\omega^2 C/R^2}{j\omega^3 R^3 C^3} - \frac{6\omega^2 C^2 R^2}{j\omega^3 R^3 C^3} \right] - \left[ \frac{j\omega^3 k\omega^3 R^3 C^3}{j\omega^3 R^3 C^3} + \frac{j\omega^3 R^3 C^3}{j\omega^3 R^3 C^3} - \frac{5j\omega^3 C}{j\omega^3 R^3 C^3} \right]}{1}$$

Khje.

$$A\beta = \frac{-j \left[ \frac{1}{\omega^3 R^3 C^3} - \frac{4k}{\omega R C} - \frac{6}{\omega R C} \right] - \left[ 3k+1 - \frac{5}{\omega^2 R^2 C^2} - \frac{k}{\omega^2 R^2 C^2} \right]}{1}$$

Replacing  $\frac{1}{\omega R C} = \omega$  for simplification so eq (14)  
Can be written as

Khje

$$A\beta = \frac{-[3k+1 - 5\omega^2 - k\omega^2] - j[\omega^3 - 4k\omega - 6\omega]}{1} \quad \dots (15)$$

To satisfy Barkhausen criterion  $\angle A\beta = 0^\circ$  hence  
imaginary part of denominator must be  $0^\circ$

$$\omega^3 - 4k\omega - 6\omega = 0$$

$$\omega [\omega^2 - (4k+6)] = 0$$

$$[\omega \neq 0]$$

$$\text{So ; } \omega^2 - (4k+6) = 0$$

$$\omega^2 = 4k+6 \Rightarrow \omega = \sqrt{4k+6}$$

Now replace  $\omega$  by  $\frac{1}{\omega R C}$  we can write.

$$\frac{1}{\omega R C} = \sqrt{4k+6} \Rightarrow \omega = \frac{1}{R C \sqrt{4k+6}}$$

$$\therefore \omega = \frac{1}{R C \sqrt{4k+6}}$$

$$\text{and } f = \frac{1}{2\pi R C \sqrt{4k+6}}$$

(16)